

## Technical Sessions Monday, September 14 – Wednesday, September 16

### Session 1 – Keynote Presentation

Oak Ballroom, Monday Morning, September 14

8:15 am

**Welcome and Opening Remarks**

**Awards Presentations**

**Keynote Speaker Introduction**

David Nairn, General Chairman

Keynote Presentation

**Another Inconvenient Truth: Snails Are More Intelligent Than Us**

Dr. Thomas Williams, Synopsys Fellow, Synopsys, Inc.

For decades there has been a new CMOS technology node approximately every two years. Until recently, thanks to scaling, the key feature of every new technology node has been a 100% integration capacity and 40% performance improvement... free-of-charge. The International Technology Roadmap for Semiconductors (ITRS) has been architected in such a way that this improvement became a self-fulfilling prophecy of the roadmap itself. Everything else has been bent in the attempt to make scaling happen... forever.

For eons snails have built the cells of their shell according to the Fibonacci's numbers: 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610, 987, etc. – where each cell has a volume that is the sum of the volume of the previous two cells. Snails understand, however, that at a certain point in time growth must stop to prevent the collapse of the shell by making it too big and therefore fragile. When this point is reached, snails do stop adding larger cells, and start improving the robustness of the shell.



Back to us: technology-wise, scaling has rapidly exhausted the resources of CMOS technology, which, by now, struggles to deliver any further improvement. Economy-wise, Dr. Gordon Moore once observed:

“What we end up doing is really selling real estate. We've sold area on the silicon wafer for about a billion dollars an acre, that order of magnitude, as long as I've been in the industry.”<sup>[1]</sup>

In order to stay afloat, the semiconductor industry would need to double the number of units it sells, from one technology node to the next. Not only is this clearly impossible, but it puts the semiconductor suppliers on a collision course with their customers, who are now looking for half the silicon area from one technology node to the next. Atoms don't scale, and markets are finite.

As decimated vanguards approach the 32-nanometer node and start planning the jump to the 22-nanometer node, a number of fundamental challenges are emerging, both technical and financial, which force a thorough rethinking of how scaling has been done, and whether scaling continues to be the most appropriate solution to provide the world with the silicon content that it needs.

Like Al Gore's premise on energy consumption and global warming, there is an inconvenient truth to be acknowledged in our industry: scaling is like fossil fuels – the cheapest and easiest way to go. Unfortunately, also like fossil fuels, it is not sustainable indefinitely. And it becomes more costly and inefficient every day. New avenues, which are available today, are worth exploring and must be undertaken. That is, unless snails are more intelligent than us...

In this keynote, Dr. Williams will describe the problems with scaling and a number of possible solutions, including the latest alternative paths and their relative merits.

### Session 2 – Over-Sampled Data Converters

Monday Morning, September 14

Oak Ballroom

Chair: Pavan Hanumolu, Oregon State University

Co-Chair: Alessandro Piovaccari, Silicon Laboratories

Four new unconventional techniques to enhance the performance of delta-sigma data converters are presented. Zero-crossing based integrators; SAR quantizers, calibration techniques, and a PWM/PDM modulator are employed.

10:00 **Introduction**

10:05 **A 630 $\mu$ W Zero-Crossing-Based  $\Delta\Sigma$  ADC Using Switched-Resistor Current Sources in 45nm CMOS**, *Tawfiq Musah, Sunwoo Kwon\*, Hasnain Lakdawala\*, Krishnamurthy Soumyanath\* and Un-Ku Moon, Oregon State University, Corvallis, OR, \*Dongbu HiTek, Seoul, Korea \*\*Intel Corporation, Hillsboro, OR*

A delta-sigma ADC employs zero-crossing-based integrators to achieve low power operation at 50MHz. Switched resistors are used as current sources, and a new charging scheme is proposed to reduce overshoot. Test chip implemented in a 45nm CMOS achieves 54.3dB DR, 52.5dB SNR, and 47.7dB SNDR at 0.833MHz while dissipating 0.63mW.

10:30 **A Low-Power 1.92MHz CT  $\Delta\Sigma$  Modulator With 5-bit Successive Approximation Quantizer**, *Mohammad Ranjbar, Arash Mehrabi and Omid Oliaeim, University of Massachusetts, Amherst, MA*

CT Delta-Sigma modulators provide a solution for low-power analog to digital conversion with built in anti-aliasing but they are sensitive to clock jitter. One way of mitigating the jitter problem is to use a multi-bit quantizer with increased number of bits. The limiting factors are quantizer delay and exponential growth of power and complexity. This paper reports the use of a 5-bit successive approximation ADC in a wide-band CT delta-sigma. The ADC structure allows easy integration of the delay compensation mechanism with minimum hardware and power. The design is implemented in a 130nm CMOS technology and measurement results show a 62 dB dynamic range and 3.1mw power consumption from a 1.2v supply.

10:55 **A Self-Calibrated 2-1-1 Cascaded Continuous-Time  $\Delta\Sigma$  Modulator**, *Junpei Kamiishi, Yun-Shiang Shu\*, Koji Tomioka, Koichi Hamashita and Bang-Sup Song\*, Asahi Kasei Microsystems, Atsugi, Japan, \*University of California, San Diego, CA*  
2-3

A 2-1-1 cascaded continuous-time delta-sigma modulator is self-calibrated with LMS-based adaptation. Exact noise cancellation filter is derived using a parameter-based continuous-time to discrete-time transform. A 0.18-micrometer CMOS prototype demonstrates a leakage noise spectral density below 10nV/ $\sqrt{\text{Hz}}$  after the capacitors in the Gm-C loop filters are self-trimmed with a 1.1%step.

11:20 **A 120dB Dynamic Range 400mW Class-D Speaker Driver with 4<sup>th</sup>-order PWM Modulator**, *Minsheng Wang, Xicheng Jiang, Jungwoo Song and Todd Brooks, Broadcom Corporation, Irvine, CA*  
2-4

A 400mW class-D speaker driver is implemented in 65nm CMOS technology, using a 4th-order digital PWM modulator to eliminate the DAC and minimize the effect of analog imperfection. It achieves 120dB dynamic range with up to 88% power efficiency while driving an 8 ohm speaker load.

### Session 3 – Biomedical Electronics

Monday Morning, September 14  
Fir Ballroom

Chair: Ed Lee, Alfred Mann Foundation

10:00 **Introduction**

10:05 **Ultra-low-power Electronics for Medicine**, *Rahul Sarpeshkar, Massachusetts Institute of Technology*  
3-1

I shall describe techniques and examples for using subthreshold analog and bio-inspired processing for creating ultra-low-power wireless electronics for the deaf, blind, paralyzed, and in other bio-signal sensing or stimulating applications. Such techniques can yield more than order of magnitude power reductions while maintaining high levels of robustness to several sources of noise. They also maintain a good amount of flexibility if they are combined with more traditional digital electronics in a synergistic fashion such that one can exploit the best of the analog and the digital worlds.

10:40 **Intracortical Microstimulation to Create Vision**, *Mohamad Sawan, University of Montreal*  
3-2

This contribution concerns a multiunit microsystem forming an intracortical implant. This bioelectronic device is dedicated for monitoring the environment of the whole implantable system as well as for microstimulation of neural tissues in order to create phosphenes representing points of light in the visual field of visually impaired person. This system includes an external controller composed of an image processing unit connected from one side to a high dynamic range image pixel sensor and from the other side to a power amplifier which is used to transmit power and data to the implant and to receive from the latter the monitored data. Several innovative circuit techniques and system assembly were applied in order to meet the application requirement in building a highly flexible system in term of feature and to reduce the needed power to operate the multiunit implant. On the other hand, integration of mixed-signal circuits and assembly of custom CMOS dies on top of electrode arrays represent one of challenging facts of the proposed devices. In addition, a full duplex high data throughput is integrated to the system, where the downlink is being based on QPSK modem method, and combined with LSK technique for the uplink transmission. System overview altogether with experimental results will be presented.

11:15 **Electronic Point-of-Care Medical Diagnostic Devices**, *Bernard Boser, University of California, Berkeley*  
3-3

Quantification of biological and biomedical processes plays a crucial role in early and acute detection of disease, food safety, and monitoring the environment. Present solutions are largely based on a complex laboratory infrastructure. Point-of-care devices (POC) based on lateral flow and colorimetric readout offer much faster turnaround time and are enjoying increasing popularity. Unfortunately the range of presently available POC solutions is limited and present devices suffer from low sensitivity.

We discuss a new class of devices based on electronic detection that overcome the shortcomings on present POC technology by offering the same ease of use, accuracy, and economy we have come to expect from consumer electronic devices. The devices duplicate the biochemistry used in laboratory tests but replace enzymatic tags with micron-scale magnetic tags attached to receptor molecules to facilitate electronic detection with integrated circuits.

11:50 **Wireless Interfaces to the Central and Peripheral Nervous System**, *Prof. Reid Harrison, University of Utah*  
3-4

The goal of the Integrated Neural Interface Project (INIP) at the University of Utah is to develop wireless, implantable devices capable of neural recording and stimulation. To this end, we have developed low power integrated circuits that can be bonded directly to a

micromachined array of silicon electrodes. The recording chip amplifies 100 weak neural signals, detects spikes with programmable threshold-crossing circuits, and returns these data via digital radio telemetry. The stimulating chip has the ability to drive 100 individual stimulation electrodes with constant-current pulses of varying amplitude, duration, interphasic delay, and repetition rate. We stimulate tissue using biphasic current pulses that inject and retract charge from the nervous system. Both chips receive power, clock, and command signals through a coil-to-coil inductive link, and require only two off-chip capacitors for operation. We have tested both chips in wireless *in vivo* experiments, recording neural signals from both nerve and cortex, and stimulating nerve fibers to elicit muscle activity and to produce evoked potentials in cortex.

#### Session 4 - Nanoscale Power and Performance Optimizations

Monday Morning, September 14  
Pine Ballroom

Chair: Osamu Takahashi, IBM  
Co-Chair: Michael Seningen, Intrinsicity

As designs migrate to nanoscale geometries, power and performance tradeoffs become critical considerations for silicon designers. The papers in this session illustrate such novel concepts and techniques.

10:00           **Introduction**

10:05           **Design Optimizations for Reduced Power and Higher Operating Frequency in a Custom x86-64 Processor Core**,  
4-1           *William Keshlear, Spence Oliver, Robert Colyer, Jeremy Schreiber, Ted Antoniadis, Tom Mickelson, Tim Puzey and Michael Bates, Advanced Micro Devices, Inc., Austin, TX*

This paper describes the methodology and tools used to drive static and dynamic power savings while significantly improving the operating frequency of a 45 nm custom x86-64 processor core used in several multi-core devices. The power improvements were essential for future six-, eight-, and twelve-core server processors, but notable improvements have already been observed in the four-core, 2.7-GHz server product and the four-core, 3.0-GHz client product.

10:30           **A Minimum Decap Allocation Technique Based on Simultaneous Switching for Nanoscale SoC**, *Kenji Shimazaki and*  
4-2           *Takaaki Okumura, Semiconductor Technology Academic Research Center*

In this paper, we propose a novel decoupling capacitance (decap) optimization technique based on simultaneous cell switching activity at the pre-layout stage. White space in the form of cell padding for the required quantity of decap is added to cells which simultaneously switch during the peak noise period, which is quickly estimated using initial timing information and the current waveforms for each cell instance, without the need to reference the power grid. The method is applied to an actual 45nm LSI and results show a 35% decap area reduction or 21.9% peak noise reduction compared with conventional decap insertion flows. The technique can improve the reliability of SoC with a runtime overhead of only 4.69% at the P&R stage in existing nanoscale SoC EDA design flows.

10:55           **Charge-Borrowing Decap: A Novel Circuit for Removal of Local Supply Noise Violations**, *Xiongfeng Meng, Resve Saleh*  
4-3           *and Steve Wilton, University of British Columbia, Vancouver, Canada*

We propose a novel circuit called charge-borrowing decap as a drop-in replacement for passive decaps to reduce supply noise for removal of "hot-spot" IR-drop problems found late in the design process. Measurement results on a 90nm test chip show that a noise reduction improvement between 42%-55% at 100MHz-1.5GHz over its passive counterpart.

11:20           **Circuit Techniques for Enhancing the Clock Data Compensation Effect under Resonant Supply Noise**, *Dong Jiao, Jie*  
4-4           *Gu and Chris Kim, University of Minnesota, Minneapolis, MN*

Recent publications have shown that clock jitter can improve timing margin through the compensation effect between the clock cycle and the data path delay under the influence of resonant supply noise. In this paper, novel phase-shifted clock buffer designs are proposed to enhance this "beneficial jitter effect". Compared with existing designs, our design saves 85% of the clock buffer area while achieving a similar 10% increase in maximum operating frequency for typical pipeline circuits. Measurement results are presented from a test chip implemented in a 1.2V, 65nm process.

11:45           **Switched Resonant Clocking (SRC) Scheme Enabling Dynamic Frequency Scaling and Low-Speed Test**, *Katsuyuki*  
4-5           *Ikeuchi, Kosuke Sakaida, Koichi Ishida, Takayasu Sakurai and Makoto Takamiya, The University of Tokyo, Tokyo, Japan*

A novel Switched Resonant Clocking (SRC) scheme is proposed to solve two basic problems of the conventional resonant clocking, that is, power increase and clock wave form instability at the lower clock frequency region. The power increase prohibits widely-used dynamic frequency scaling (DFS) and the wave form instability hinders low-speed function tests. A test chip in 0.18 $\mu$ m CMOS is manufactured and measured to show that the SRC suppresses power increase at low clock frequency and enables the low-speed tests, while reducing the clock power by 8% at 1.5-GHz clock with an area penalty of 4.8%.