MONDAY Morning Program

Session 1 – Keynote Presentation

Monday Morning, September 20
Oak Ballroom
8:15am

Welcome and Opening Remarks
Awards Presentations
Keynote Speaker Introduction
Rakesh Patel, General Chairman

Keynote Presentation
James D. Meindl
Nanotechnology Research Center & School of Electrical and Computer Engineering,
Georgia Institute of Technology, Atlanta, GA

Since 1960 silicon microchip technology has advanced in productivity by the astounding factor of one billion times. Concurrently, the performance of microchips, for example a microprocessor chip, has increased by a factor of approximately one million times since the early 1970's. These two concurrent advances are unmatched in technological history. The salient objective of this discussion is to provide an incisive response to the question: what's next?

Reducing the minimum feature size (F) of transistors and interconnects in a microchip or scaling has been the single most potent factor enabling the huge improvements in both productivity and performance of microchips during the past half century. To be more specific, transistor printed gate length has been scaled from 25 µm to 25nm or by a factor of 1000x. However, within the next decade limitations such as gate tunneling current and subthreshold drain-to-source current will demand the introduction of new high permittivity gate insulators and metal gates. These new materials and new device structures such as the vertical FinFET will be necessary to enable continued scaling albeit at a substantially reduced rate. A transition from 193 nm optical lithography to EUV technology will also be necessary to support scaling to the sub-10nm region.

As the advance of intrinsic silicon technology nears a saturation point in the sub-10nm range, opportunities for ancillary technology and especially for three-dimensional (3D) integration will become vigorously pursued. Stacking of low power flash memory chips is now a production technology but stacks of microprocessor and memory chips, for example, in a high performance multi-core processor are not yet in use particularly due to heat removal limitations. However, promising innovative approaches to electrical interconnection and liquid cooling of a stack using electrical and fluidic through-silicon vias have been presented.

Beyond another decade of silicon technology advances, perhaps the most promising prospect that is under intense investigation is graphene, particularly due to its ballistic carrier transport, adjustable energy band gap of nanoribbons and potential for fusion of top-down and bottom-up nanotechnology.

Session 2 -Enhanced Modeling Techniques

Monday Morning, September 19
Oak Ballroom

Chair: Colin McAndrew, Freescale Semiconductor
Co-Chair: Hidetoshi Onodera, Kyoto University

This session presents recent developments in nanowire transistor modeling, on-chip transformer and balun modeling, reliability modeling of large digital systems, and wafer-specific model centering.

10:00 AM **Introduction**

10:05 AM
2-1 **Characterization and Analysis of Gate-All-Around Si Nanowire Transistors for Extreme Scaling (INVITED),** *Ru Huang, Runsheng Wang, Jing Zhuge, Changze Liu, Tao Yu,Liangliang Zhang, Xin Huang, Yujie Ai, Jinbin Zou, Yuchao Liu, Jiewen Fan, Huailin Liao, Yangyuan Wang, Peking University*

The gate-all-around Si nanowire transistor is one of the best candidates for ultimately scaled CMOS devices at the end of roadmap. This paper reviews our recent work on characterization and analysis of this unique device from experiments and simulation, including carrier transport, parasitics, noise, self-heating, variability and reliability, which can provide useful information for the nanowire device hierarchical modeling and device/circuit co-design.

10:55 AM
2-2 **Broadband Compact Model for On-Chip mm-Wave Transformers and Baluns with Emphasis on Capacitive Coupling Effects,** *Yang Tang, Zuochang Ye, Yan Wang, Tsinghua University*

Distributed capacitive coupling effects in the transformers and baluns at millimeter-wave band are investigated in this paper and a lumped coupling branch with parameter estimation method is proposed. The accuracy near and beyond resonance frequency of the new equivalent circuit model is greatly improved. Different types of transformers and baluns with various geometries are fabricated by 0.13um RF CMOS process. The model agrees quite well with all the experiments up to 40GHz and further validated by EM simulations up to 80GHz, indicating that it captures the physical essence behind correctly.

11:20 AM
2-3 **Bottom-Up Digital System-Level Reliability Modeling,** *N. Ruiz Amador, V. Huard, E. Pion, F. Cacho, D. Croain, V. Robert, S. Engels, P. Flatresse, L. Anghel* ,STMicroelectronics, *TIMA Laboratory*

In this paper we demonstrate that it is possible by a bottom-up approach to build transistor-and gate-level models with enough accuracy to allow direct comparison with experimental degradations at system-level.

11:45 AM
2-4 **Wafer-Specific Centering of Compact Transistor Model Parameters for Advanced Technologies and Models.,** *B. De Vries, A.J. Scholten, P.F.E. Rommers*, M. Stoutjesdijk*, and D.B.M. Klaassen, NXP Central R&D Research, *NXP Central R&D Foundation Technology*

For older technologies and compact models it is often possible to directly calculate a compact model parameter set based on a limited amount of process-control module measurements. For advanced technologies and surface-potential-based compact models this is no longer the case. Here, we present a novel method to restore this capability.

Session 3 - Clock Synthesis and CDRs

Monday Morning, September 19
Fir Ballroom

Chair: William Walker, Fujitsu Laboratories of America
Co-Chair: Shunichi Kaeriyama, Renesas Electronics Corporation

This session covers low-skew multi-phase clock generation, a PLL synthesized from a standard cell library, and digital techniques for clock and data recovery.

10:00 AM **Introduction**

10:05 AM
3-1
Area Efficient Phase Calibration of a 1.6 GHz Multiphase DLL, *Ankur Agrawal, Pavan Kumar Hanumolu*, Gu-Yeon Wei**, IBM Research, *Oregon State University, **Harvard University*

This paper describes a digital calibration scheme that corrects for phase spacing errors in a multiphase clock generating delay-locked loop (DLL). The calibration scheme employs sub-sampling using a frequency-offset clock with respect to the DLL reference clock, to measure phase-offsets. The phase-correction circuit uses one digital-to-analog converter across eight variable-delay buffers to reduce the area consumption by 62%. The test-chip, designed in a 130nm CMOS process, demonstrates a 8-phase 1.6 GHz DLL with a worst-case phase error of 450fs.

10:30 AM
3-2
Digital Clock and Data Recovery Circuit Design: Challenges and Tradeoffs, *Mrunmay Talegaonkar, Rajesh Inti, and Pavan Kumar Hanumolu, Oregon State University*

Digital clock and recovery circuits (CDRs) have recently emerged as an alternative to their more classical analog counterparts. This paper seeks to elucidate the design challenges and trade-offs involved in the design of digital CDRs. The jitter performance metrics such as jitter generation, jitter transfer, and jitter tolerance are related to digital CDR parameters and design guidelines are provided. The impact of digital phase detector non-linearity and quantization error, the digitally-controlled oscillator frequency quantization error, and loop latency on a digital CDR performance is analyzed and demonstrated using accurate behavioral simulations.

11:20 AM
3-3
An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS, *Y. Park, D. Wentzloff, University of Michigan*

This paper presents an all-digital PLL (ADPLL) in which all functional blocks have been synthesized from standard digital cells and automatically placed and routed (P&R). A calibration scheme is proposed to account for the systematic mismatch resulting from P&R. The ADPLL is fabricated in 65nm CMOS and occupies 0.042mm2. The period jitter is 3.2psrms (36pspp) at 2.5GHz, and the power consumption is 9.1mW to 14.6mW over a 1.5 to 2.7GHz frequency range.

11:45 AM
3-4
An Open-Loop 10GHz 8-Phase Clock Generator in 65nm CMOS, *X. Yang, J. Liu, University of Texas at Dallas*

An open-loop 10GHz 8-phase clock generator is presented. It is composed of delay units and phase interpolators with built-in phase compensation for delay variation. A delay unit design with level-shifted active inductor load enables the circuit to achieve 10GHz speed with 0.19mW/GHz/phase power efficiency in 65nm CMOS.

Session 4 – Wireless Transceivers in CMOS

Monday Morning, September 19
Pine Ballroom

Chair: Julian Tham, Broadcom
Co-Chair: Ramesh Harjani, University of Minnesota

Wireless transceiver designs for software defined radio, GPS, wireless headphones and sensors nodes are presented. Implementations range from 40nm to 180nm CMOS technology nodes.

10:00 AM **Introduction**

10:05 AM 4-1 **SAW-less Software-Defined Radio Transceivers in 40nm CMOS (INVITED),** *Jan Craninckx, Jonathan Borremans, Mark Ingels, IMEC*

The introduction of several new cellular and connectivity radio standards has attracted the wireless industry to the concept of software-defined radio systems, preferably implemented in advanced nanometer CMOS technology. A first generation of transceivers, using several advances in new circuits and architectures, combined with extensive digital compensation techniques, are indeed able to operate over the complete range of both RF frequencies and baseband bandwidths and as such act like an SDR. However, a real SDR must go further than this. Interoperability and coexistence scenarios, combined with the need to eliminate external fixed-frequency acoustic RF filters, lead to much more stringent requirements on linearity and noise. Therefore, this paper will also present a novel second generation of 40nm CMOS transceivers that enable this. On the TX side, it is crucial to achieve -160dBc/Hz noise level for all possible combinations of RF frequency, baseband bandwidth, and RX-TX duplex spacing. In the receiver, extremely linear circuits are presented, that are able to handle blockers of around 0dBm input level.

10:55 AM 4-2 **A Dual-Channel GPS/Compass/Galileo/GLONASS Reconfigurable GNSS Receiver in 65nm CMOS,** *Nan Qi, Yang Xu, Baoyong Chi, Yang Xu, Xiaobao Yu, Xing Zhang, Zhihua Wang, Tsinghua University*

A fully-integrated dual-channel reconfigurable GNSS receiver supporting GPS/Compass/Galileo/GLONASS in 65nm CMOS is presented. The receiver has two independent channels to support simultaneous reception. One frequency synthesizer is shared by two channels to avoid LO crosstalk. The receiver achieves 2.2dB noise figure, 50dB IRR on average, while consuming minimum 31mW power.

11:20 AM 4-3 **Complete SOC Transceiver in 0.18µm CMOS using Q-enhanced Filtering, Sub-sampling and Injection Locking,** *R. Mason, J. Fortier*, C. DeVries**, SMSC, *Hittite Microwave Corporation, **Research in Motion*

Portable wireless headphones have not been widely accepted. The main reasons for this are that power consumption is too high and interference management is poor. A workable wireless headphone is presented. The transceiver is fabricated in 0.18µm CMOS and consumes peak RX/TX currents of 10.2mA and 22mA respectively.

11:45 AM 4-4 **A Wireless Sensor Node for Condition Monitoring Powered by a Vibration Energy Harvester,** *J. Jang, D.F. Berdy, J. Lee, D. Peroulis, B. Jung, Purdue University*

A complete duty-cycle controlled, FDMA and TDMA compatible wireless condition monitoring sensor node with 85.5 µW measured average power consumption is presented with a high level of integration. It is experimentally demonstrated to operate autonomously from the power provided by a piezoelectric vibration energy harvester.

Session 5 – Technology and Circuit Drivers for Ultra-Scale CMOS

Monday Morning, September 19
Cedar Ballroom

Chair: Rajiv Joshi, IBM TJ Watson Research Center
Co-Chair: Kingsuk Maitra, GlobalFoundries

This session of invited papers covers key technology and circuit drivers such as process variability, interconnect delays, tower management, memory functionality, and reliability for marching towards 15nm CMOS.

10:00 AM **Introduction**

10:05 AM
5-1
15nm Design and Technology Interaction Beyond (INVITED), *M. Clinton, C. Bittlestone, V. Menezes, V. Le, G. Girishankar, Texas Instruments*

Abstract-This paper will discuss the challenges that continued technology scaling present to circuit designers and how the close interaction between the development of technology, design automation (EDA) tools and the circuit designer can overcome these challenges and enable designs that deliver the benefits customers expect from continued technology scaling

10:55 AM
5-2
Statistical Advantages of Intrinsic Channel Fully Depleted SOI MOSFETs over Bulk MOSFETs (INVITED), *Toshiro Hiramoto, Anil Kumar, Tomoko Mizutani, Jun Nishimura, Takuya Saraya, University of Tokyo*

Statistical characteristics of intrinsic channel FD SOI MOSFETs and conventional bulk MOSFETs are compared. It is experimentally shown that not only Vth variability but DIBL and current onset voltage (COV) variability is well suppressed in FD SOI MOSFETs. Moreover, Vth change due to random telegraph noise (RTN) is also smaller in FD SOI MOSFETs. It terms out that the absence of random dopant fluctuation (RDF) is responsible for the suppressed variability.

11:20 AM
5-3
28nm Metal-gate High-K CMOS SoC Technology for High-Performance Mobile Applications (INVITED), *S.H. Yang, J.Y. Sheu, M.K. Ieong, M.H. Chiang, T. Yamamoto, J.J. Liaw, S.S. Chang, Y.M. Lin, T.L. Hsu, J.R.Hwang, J.K. Ting, C.H. Wu, K.C. Ting, F.C. Yang, C.M. Liu, I.L. Wu, Y.M. Chen, S.J. Chent, K.S. Chen, J.Y. Cheng, M.H Tsai, W. Chang, R. Chen, C.C. Chen, T.L. Lee, C.K Lin, S.C. Yang, Y.M. Sheu, J.T. Tzeng, L.C. Lu, S.M Jang, C.H. Diaz, YJ Mii, Taiwan Semiconductor Manufacturing Company*

An industry leading 28nm high-performance mobile SoC technology featuring metal-gate/high-k process is presented. The technology is optimized to offer wide power-to-performance transistor dynamic range and highest wired gate density with superior low-R/ELK interconnects, critical for next generation mobile computing/SOC applications. Through process and design optimization, historical trend is maintained for gate density and SRAM cell sizes. Variations control strategy through process and design collaboration is also described.