Technical Sessions
Monday, September 20 - Morning

Session 1 – Keynote Presentation

Monday Morning, September 20
Oak Ballroom

8:15 **Welcome and Opening Remarks**

Awards Presentations

Keynote Speaker Introduction
Jacqueline Snyder, General Chairman

Keynote Presentation
Green Chips: A New Era for the Semiconductor Industry
René Penning de Vries, NXP Semiconductors

The need to minimize the use of fossil fuels to generate electrical energy has been the topic of extensive discussions in the last couple of years. Next to replacement of fossil fuels by alternatives, there is increasing awareness that scrutiny of existing technology and applications can have an immediate, and profound impact. In the presentation the focus will be on the use of high performance mixed signal technologies to minimize energy usage in various applications, such as static and dynamic power of chargers, lighting by CFL and LED technique, as well as various applications in the car.

René Penning de Vries is Senior Vice President and Chief Technology Officer of NXP Semiconductors BV. René is responsible for the product creation processes at NXP, focusing on the key areas of innovation, technology and research. René previously held the position of CTO at Philips Semiconductors prior to the formation of NXP in 2006. He started working for Philips Research in 1984. His career evolved from various technical and managerial roles in CMOS development, into management of platform and design technology as well IP creation. Later, system technology and research were added to his portfolio. During his career, René worked and lived in the US, France and in Singapore, where he was VP of Technology in SSMC.

Session 2 – Advanced Embedded Memories

Monday Morning, September 20
Oak Ballroom

Chair: Vikas Chandra, ARM
Co-Chair: Muhammad Khellah, Intel Corporation

Several new DRAM and SRAM approaches are presented. High speed DRAM, SRAM with Vmin and read/write stability improvement, low energy consumption are discussed.

10:00 **Introduction**

10:05
02-1
A 45nm SOI Compiled Embedded DRAM with Random Cycle Times Down to 1.3ns (INVITED), *Mark Jacunski, Darren Anand, Robert Busch, John Fifield, Matthew Lanahan, Paul Lane, Adrian Paparelli, Gary Pomichter, Dale Pontius, Michael Roberge, Stephen Sliva, IBM Systems and Technology Group*

A family of eDRAMs fabricated in 45nm SOI technology is presented. The fast eDRAM has 64 b/BL and achieves a random cycle time of 1.3ns for VDD=1.0V and typical process. The dense eDRAM has 128 b/BL and operates in multi-bank modes up to 1.67GHz.

10:30
02-2
Improving SRAM Vmin and Yield by Using Variation-aware BTI Stress, *Jiajing Wang, Satyanand Nalam*, Zhenyu Qi*, Randy Mann*, Mircea Stan*, Benton Calhoun*, Intel Corporation, *University of Virginia*

We propose a novel method that exploits BTI to partially offset variation and thus improve SRAM Vmin and yield. We show correlation between a bitcell's power-up state and its static noise margin. By applying stress with periodic re-power-up, device mismatch can be compensated by BTI induced changes. The proposed method has no extra design and area cost. It can be applied during burn-in test to offset manufacturing variation and/or used during the lifetime of the chip to offset variation from real-time aging and hence continue to improve the margins. Simulations in 45nm show that write, read, and hold Vmin at 6σ can be reduced by 128, 75, and 91 mV, respectively. Measurements from a 16Kb 45nm SRAM demonstrate the improvement of Vmin and yield.

10:55
02-3
Technology-Circuit Co-Design of Asymmetric SRAM Cells for Read Stability Improvement, *Jae-Joon Kim, Rahul Rao, Keunwoo Kim, IBM T. J. Watson Research Center*

We present asymmetric SRAM cell design approaches to improve read stability over conventional symmetric SRAM Cell. We show that selective threshold voltage control is more effective than adjusting transistor size for read stability improvement in an asymmetric SRAM cell. We implement statistical DC noise margin monitors and present the hardware measurement data as well as the DC/AC simulation data to support the claims.

11:20
02-4
7T SRAM Enabling Low-Energy Simultaneous Block Copy, *Shunsuke Okumura, Shusuke Yoshimoto, Kosuke Yamaguchi, Yohei Nakata, Hiroshi Kawaguchi, Masahiko Yoshimoto, Kobe University*

This paper proposes a 7T SRAM that implements block-level simultaneous copying feature. The proposed SRAM can be used for data transfer between local memories such as checkpoint data storage and transactional memory. In the proposed SRAM, 16-kb data can be copied in 33.3 ns at 1.2V. The proposed scheme reduces energy consumption in copying by 92.7% compared to the conventional read-modify-write manner.

11:45
02-5
A 32nm 0.5V-Supply Dual-Read 6T SRAM, *Jente Kuang, Jeremy Schaub, Fadi Gebara, Dieter Wendel, Sudesh Saroop, Tuyet Nguyen, Thomas Fröhnel, Antje Müller, Christopher Durham, Rolf Sautter, Bryan Lloyd, Bryan Robbins, Jürgen Pille, Sani Nassif, Kevin Nowka, IBM*

We report a high-performance dual read port 8-way set associative 6T SRAM with a one clock cycle access latency, in a 32nm metal-gate partially depleted (PD) SOI technology, for low-voltage applications. The hardware exhibits robust operation at 348MHz and 0.5V with a read and write power of 3.33 and 1.97mW, respectively, per 4.5KB active array with both read ports accessed at the highest activity data pattern. At 0.6V, an access speed of 1.2GHz is observed.

Session 3 – Technology Variability Modeling

Monday Morning, September 20
Fir Ballroom

Chair: Colin McAndrew, Freescale Semiconductor, Inc.
Co-Chair: Frank Liu, IBM Austin Research Lab

Statistical modeling of device mismatch and variability is critical in scaled integrated circuits.

10:00 **Introduction**

10:05
03-1
Modeling and Simulation of Transistor and Circuit Variability and Reliability (INVITED), *Asen Asenov, Binjie Cheng, Daryoosh Dideban, Urban Kovac, Negin Moezi, Campbell Millar, Gareth Roy, Andrew Brown, Scott Roy, University of Glasgow*

Statistical variability associated with discreteness of charge and granularity of matter is one of limiting factors for CMOS scaling and integration. The major MOSFET statistical variability sources and corresponding physical simulations are discussed in detail. Direct statistical parameter extraction approach is presented and the scalability of 6T and 8T SRAM of bulk CMOS technology is investigated. The standard statistical parameter generation approaches are benchmarked and a newly developed parameter generation approach based on nonlinear power method is outlined.

10:55
03-2
Technology Variability from a Design Perspective (INVITED), *Borivoje Nikolić, Bastien Giraud, Zheng Guo*, Liang-Teck Pang**, Ji-Hoon Park, Seng Oon Toh, University of California, Berkeley, *Intel Corp, **IBM T.J. Watson Research Center*

Increased variability in process technology and devices requires added margins in the design to guarantee the desired yield. Variability is characterized with respect to the distribution of its components, spatial and temporal characteristics and impact on specific circuit topologies. Approaches to variability characterization and modeling for digital logic and SRAM are reviewed in this paper. Transistor and ring oscillator arrays are designed to isolate specific systematic and random variability components in the design. Distributions of SRAM design margins are measured by padded-out cells and minimum operating voltages for the entire array. Correlations between various components of variability are essential for adding appropriate margins to the design.

11:45
03-3
Statistical Modeling and Post Manufacturing Configuration for Scaled Analog CMOS, *Gokce Keskin, Jonathan Proesel, Larry Pileggi, Carnegie Mellon University*

Process variations in advanced CMOS process nodes limit the benefits of scaling for analog designs. In the presence of increasing random intra-die variations, mismatch becomes a significant design challenge in circuits such as comparators. In this paper we describe and demonstrate the details of a statistical element selection (SES) methodology that relies on choosing a subset of selectable circuit elements (e.g., input transistors in a comparator) to achieve the desired specification (e.g., offset). Silicon results from a 65nm test chip demonstrate that SES can achieve an order of magnitude better matching than both redundancy and Pelgrom-model sizing given the same core circuit area.

Session 4 – Advanced and Specialty IC Technologies

Monday Morning, September 20
Pine Ballroom

Chair: Takamaro Kikkawa, Hiroshima University
Co-Chair: Rich Liu, Macronix International, Co., Ltd.

This session discusses challenges in 3D IC integration, monitoring and managing process variability, and foundry issues beyond mainstream IC technology.

10:00 **Introduction**

10:05
04-1
Three-Dimensional Integration Technology Using Through-Si Via Based on Reconfigured Wafer-to-Wafer Bonding (INVITED), *Mitsumasa Koyanagi, Takafumi Fukushima, Tetsu Tanaka, Tohoku University*

Three-dimensional (3-D) integration technologies using through-silicon vias (TSV's) are described. We have developed a 3-D integration technology using TSV's based on a wafer-to-wafer bonding method for the fabrication of new 3-D LSIs. A 3-D image sensor chip, 3-D shared memory chip, 3-D artificial retina chip and 3-D microprocessor test chip have been fabricated by using this technology. In addition, we have developed a new 3-D integration technology based on a reconfigured wafer-to-wafer bonding method called a super-chip integration. A number of known good dies (KGDs) are simultaneously aligned and bonded onto lower chips or wafers with high alignment accuracy by using a new self-assembly technique in a super-chip integration.

10:55
04-2
Analyzing the Impact of Double Patterning Lithography on SRAM Variability in 45nm CMOS, *Vivek Joshi, Michael Wieckowski, Gregory Chen, David Blaauw, Dennis Sylvester, University of Michigan*

This paper analyzes the impact of double patterning lithography (DPL) on 6T SRAM variability. A test chip is implemented in a 45nm CMOS process that uses DPL. Measurements from 75 die demonstrate a significant impact of DPL on SRAM failures. Extensive analysis demonstrates that DPL induced mismatch considerably increases functional failures in SRAM cells, and degrades yield. We also propose a DPL-aware sizing technique to mitigate yield losses.

11:20
04-3
Parameter-Specific Ring Oscillator for Process Monitoring at the 45 nm Node, *Lynn Wang, Nuo Xu, Seng Oon Toh, Andrew R. Neureuther, Tsu-Jae King Liu, Borivoje Nikolic, University of California, Berkeley*

Parameter-specific ring oscillator (RO) experimental results are reported, demonstrating the ability to electronically distinguish and quantify sources of variations from gate lithography focus, gate-to-active overlay, nitride contact etch stop layer (CESL) strain, and shallow trench isolation (STI) stress. A 2% RO frequency change due to gate focus variations, a three-four nm overlay error, a 20% increase in RO frequency per 1 um increase in length of diffusion (LOD), and a 3% speed-up per 0.3 um change in STI width are measured. Typical standard-deviation/mean (σ/μ) among 36 ROs within-chip is 0.2-0.3%.

11:45
04-4
Specialty Foundry Technology and Design Enablement for RF, High Performance Analog, and Power (INVITED), *Samir Chaudhry, Marco Racanelli, TowerJazz*

The large customer breadth of the Specialty Foundry is driving process technology and design enablement innovation that is hard to replicate within an integrated device manufacturer (IDM) which serves a more focused customer base. In this paper we will review Specialty Foundry technology in the areas of RF, high-performance analog, and power. We will also review novel design enablement tools available from the Specialty Foundry that leverage the tight interaction between EDA, models, and process technology to improve time to market and yield of highly integrated analog products.

Session 5 – RF Transceivers

Monday Morning, September 20
Cedar Ballroom

Chair: Aristotele Hadjichristos, Qualcomm
Co-Chair: John Rogers , Carleton University

This session will present explosive advances in transceivers for an epic range of applications spanning over 100GHz of spectrum. New circuit and architectural techniques are addressed.

10:00 **Introduction**

10:05
05-1 **Highly Integrated and Tunable RF Front-Ends for Reconfigurable Multi-Band Transceivers (INVITED),** *Hooman Darabi, Broadcom Corp.*

Architectural and circuit techniques to integrate the RF front-end passive components, namely the SAW filters and duplexers that are traditionally implemented off chip, are presented. Intended for software defined radios, tunable high-Q filters allow the integration of highly reconfigurable transceiver front-ends that are robust to in-band and out-of-band blockers. Furthermore, duplexer techniques based on electrical balance concept are introduced to enable highly integrated and programmable radios for full duplex applications such as 3/4G transceivers.

10:55
05-2 **A 1.2 mm^2 Fully Integrated GPS Radio with Cellular/WiFi Co-existence,** *Paul Yu, Todd Sepke, Belal Helal, Shervin Shekarchian, Danilo Gerna, Konstantinos Sarrigeorgidis, Lydi Smaini, Arnab Mitra, James Li, Brian Brunn, Greg Uehara, Thomas Cho, Marvell Semiconductor*

This paper presents a fully integrated GPS receiver with 2.4 dB NF, 1.2mm^2 area, and 13 mA of current in 55 nm CMOS. NF degrades by only 0.1/0.5/0.1 dB in the presence of GSM, DCS, and WiFi blockers respectively. By using current mode operation, push-pull topology, current reuse techniques, and modular Gm-TIA stages, the area is about half and power is about 1/3 of previously published GPS receivers while having similar or better co-existence performance.

11:20
05-3 **A Flexible 500MHz to 3.6GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21MS/s SAR ADC,** *David Lin, Li Li, Shahin Farahani*, Michael Flynn, University of Michigan, Ann Arbor, *Freescale Semiconductor*

A flexible, digital-dominant wireless receiver is implemented in 65nm CMOS. The receive chain consists of a wideband LNA, mixers, and baseband amplifiers. A 7b 21MS/s SAR ADC with embedded, configurable DT FIR/IIR filtering rejects aliasing interferers. Interleaving of sampling and SAR in the ADC maximizes the conversion rate. The receiver achieves -92dBm sensitivity, +33dB and +39dB adjacent and alternate channel interferer rejection with 802.15.4 packets, respectively, and -83dBm sensitivity, +41dB, +20MHz interferer rejection with 802.11 packets.

11:45
05-4 **D-Band CMOS Transmitter and Receiver for Giga-Bit/sec Wireless Data Link,** *Zhiwei Xu, Qun Jane Gu, Yi-Cheng Wu, Adrian Tang, Yu-Ling Lin*, Ho-Hsian Chen*, Chewnpu Jou*, Mau-*

*Chung Frank Chang, UCLA, *TSMC*

A 140GHz transmitter and receiver for Giga-Bit/sec data communication have been designed, fabricated and demonstrated in 65nm CMOS. The chip uses ASK modulation to realize this non-coherent data link and achieve compact design and low power operation. Over 2.5Gbps data link has been validated and the chipset occupies 0.03mm^2/0.12mm^2 and burns 115mW/120mW for TX/RX respectively.