

**EDUCATIONAL SESSIONS**  
Sunday, September 18

Chairperson: Ramesh Harjani, University of Minnesota

**Educational Session Track 1 – Radio Basics for Those New to Wireless Design**

Oak Ballroom, Sunday, September 18

Organizers: Ehsan Afshari, Cornell University  
Co-Organizer: Howard Luong, Hong Kong University of Science & Tech.

Recent advances in wireless technologies have transformed people's lifestyles with many portable devices such as smart-phones, laptops/tablets, personal navigation, and so on. This tutorial provides basic concepts and understanding of RF transceiver design for those who are new to this subject. Topics are divided into two parts. In the first part, basic concepts of the RF transceivers including transmitter, receiver, coexistence, etc. are presented. In the second part, development of design requirements from a specification document are presented, using a 3GPP transceiver as an example.

8:30 am - 10:20 am

**E1-1 Radio Basics for Those New to Wireless Design: Principles**

Thomas Cho, Marvell

Thomas Cho received the B.S. degree in electrical engineering from UCLA in 1989 and the M.S. and Ph.D. degrees from UC Berkeley (UCB) in 1991 and 1995, respectively. In 1995, he was with UCB as a Visiting Lecturer teaching a senior-level course on analog integrated circuits, and from 1995 to 1996, he was involved in the Multi-Standard Monolithic CMOS RF Transceiver project as a Postdoctoral Researcher. From 1996 to 2000, he was with Level One Communications, developing CMOS RF transceivers for cordless phone applications. In 2000, he co-founded Wireless Interface Technologies (WIT), developing CMOS RF transceivers for WPAN/WLAN applications, which was later acquired by Chrontel. Since 2004, he's been with Marvell semiconductor, managing several RF and analog teams to develop CMOS RF transceivers for various wireless applications such as multi-functional radio, MIMO, etc.

10:30 am - 12:20 pm

**E1-2 Radio Basics for Those New to Wireless Design: 3GPP Specification Translation**

Earl McCune, RF Communications Consulting

Earl McCune is a serial entrepreneur from Silicon Valley with over 35 years of experience in design of wireless circuits, modulations, and systems. In recent years he has focused on breaking the standard tradeoff between power amplifier linearity and energy efficiency, which led him to switch-based circuit design techniques and polar signal processing. He has more than 50 US patents granted. Having retired from industry in 2008, he now "gives back" as a visiting instructor, author, and consultant. He is a graduate of UC Berkeley, Stanford, and UC Davis.

**Educational Session Track 2 – Advanced Topics: Power Management**

Fir Ballroom, Sunday, September 18

Organizer: Raj Amirtharajah, University of California, Davis  
Co-Organizer: Hoi Lee, University of Texas at Dallas

8:30 am – 10:20 am

**E2-1 Integrated DC-DC Conversion**

Seth R. Sanders, UC Berkeley

CMOS chips have evolved to operate at steadily lower supply voltages and increasing power densities, leading to drastic reductions in the required impedance of the supply distribution network. For example, today's 1V, 100A microprocessors require a supply impedance of ~1mOhm, which is extremely challenging to achieve across a broad range of frequencies. Indeed, this impedance requirement limits the amount of current that can be efficiently delivered onto the die, limiting the ability to improve performance by integrating additional cores. Furthermore, supporting multiple independent supply voltages on the die (for improved power management) is currently very challenging due to the impedance degradation associated with heavily partitioned package power planes.

In order to overcome these challenges, in this talk we will describe fully integrated voltage converters that maximize the overall efficiency and robustness of high-performance digital chips. To allow for multiple on-chip supply voltages and simplify the board- and package-level power delivery networks, we will focus on an architecture consisting of many distributed, fully-integrated switching regulators (for efficient conversion of a single external high-voltage supply) combined with parallel linear regulators to control the AC impedance. Since the parallel linear regulator can be designed to spend minimal power in setting the effective supply impedance, the switching regulator can be optimized purely for conversion efficiency. As an additional benefit, integrating the voltage converter onto the die relaxes the impedance requirements of the global supply, potentially leading to significant simplifications in the complexity of the package and PCB power distribution networks.

Seth R. Sanders is a Professor of Electrical Engineering in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. He received S.B. degrees (1981) in Electrical Engineering and Physics, and the S.M. (1985) and Ph.D.

(1989) degrees in Electrical Engineering from the Massachusetts Institute of Technology, Cambridge. Following an early experience as a Design Engineer at the Honeywell Test Instruments Division in 1981-83, he joined the UC Berkeley faculty in 1989. His research interests are in high-frequency power conversion circuits and components, in design and control of electric machine systems, and in nonlinear circuit and system theory as related to the power electronics field. Dr. Sanders is presently or has recently been active in supervising research projects in the areas of flywheel energy storage, novel electric machine design, renewable energy systems, and digital pulse-width modulation strategies and associated IC designs for power conversion applications. During the 1992-1993 academic year, he was on industrial leave with National Semiconductor, Santa Clara, CA. Dr. Sanders received the NSF Young Investigator Award in 1993 and multiple Best Paper Awards from the IEEE Power Electronics and the IEEE Industry Applications Societies. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom. He is an IEEE Fellow.

10:30 am – 12:20 pm

**E2-2 LED Driver Circuits for Mobile Applications**

Greg Winter and Arun Rao, National Semiconductor

LEDs have become the lighting source of choice for mobile applications such as display backlights in mobile phones, tablets, and laptops and portable camera flash. The constraints of battery-powered applications require efficient DC/DC voltage conversion while delivering sufficient current to generate adequate light and simultaneously managing thermal effects. This talk reviews LED device operation for portable lighting, describes efficient switching converter architectures, and summarizes thermal design considerations.

Greg Winter is a Staff Engineer at National Semiconductor Corporation. He has a BSEE from Cal Poly San Luis Obispo and 12 years of design experience in the area of portable power, mostly for LED backlight drivers, including parallel and series architectures, inductive and switched capacitor converters, dynamic backlight control and ambient light sensing. He has additional experience with high power flash drivers.

Arun Rao is a Principal Engineer at National Semiconductor Corporation. He has an MSEE from Oregon State University and 9 years of experience designing products in the area of portable power, mostly for flash LED and backlight drivers, using both switched capacitor and inductive architectures designed in CMOS.

**Educational Session Track 3 – Analog Behavioral Modeling**

Pine Ballroom, Sunday, September 18

Organizer: Larry Nagel, Omega Enterprises Consulting

Co-Organizer: Colin McAndrew, Freescale Semiconductor, Inc.

8:30 am - 10:20 am

**E3-1 Analog Behavioral Modeling with Verilog-A**

Boris Troyanovsky, Tiburon Design Automation

Over the past several years, Verilog-A has gained widespread adoption in the area of analog behavioral modeling. In this session, we provide an overview of the Verilog-A language and illustrate its applicability to various analog modeling tasks. Examples ranging from analog system-level modeling to compact device modeling are presented, and the language's applicability to such areas as noise modeling and RF analysis are discussed.

Boris Troyanovsky received his BS degree in EECS from UC Berkeley, and MS and PhD degrees in Electrical Engineering from Stanford University. From 1995 to 2002, he was with HP's (subsequently Agilent's) EEs of division, working in the area of high-frequency circuit simulation. Since 2002, he's been with Tiburon Design Automation as co-founder/partner/CTO, working in the area of Verilog-A compiler development.

10:30 am - 12:20 am

**E3-2 Verification of Complex Analog Integrated Circuits**

Ken Kundert, Designer's Guide Consulting

Verification is becoming widely recognized as one of the most important issues when designing large complex analog and RF mixed-signal circuits. As a result, design methodologies are starting to change. This change mirrors a change that occurred in digital design 10-15 years ago. In this presentation I will show why the problem has become so significant, and what people are doing to control the problem. This presentation is targeted for design management, design engineers, and verification engineers. It outlines a practical and proven methodology for performing the complete functional verification of the most complex analog SoCs using examples to illustrate the essential points. This methodology not only assures that the implementation is functionally consistent with the specification, but it also produces a high-level Verilog or VHDL model that is shown through exhaustive transistor-level testing to be functionally equivalent to the implementation. Use of this methodology also leads naturally to the adoption of a top-down design style and aids performance verification.

Dr. Ken Kundert is President and co-founder of Designer's Guide Consulting, a company that is guiding the industry towards adoption of formalized analog verification. Previously, he worked at Cadence and HP, where he created Spectre, SpectreRF, Verilog-A/MS and HP's (now Agilent's) harmonic balance simulator. He has written three books on circuit simulation and modeling and created "The Designer's Guide Community" website. He received his Ph.D. in Electrical Engineering from the University of California at Berkeley in 1989. Ken was elevated to the status of IEEE Fellow in January 2007 for contributions to simulation and modeling of analog, RF, and mixed-signal circuits.

## Educational Session Track 4 – PLL Fundamentals

Oak Ballroom, Sunday, September 18

Organizer: Pavan Kumar Hanumolu, Oregon State University  
Co-Organizer: Shahriar Mirabassi, University of British Columbia

1:30 pm - 3:20 pm

### **E4-1 Phase-Locking Techniques for Frequency Synthesis**

Pavan Kumar Hanumolu, Oregon State University

Phase-locked loops (PLLs) are essential building blocks in all digital, analog, and radio-frequency integrated circuits (ICs). The noise, power, and area of PLLs determine many of the key performance parameters in all such ICs. This tutorial describes the fundamental principles and concepts of PLL design. After reviewing the operation of a simple type-1 PLL and the characteristics of its building blocks, the operating and design principles of a charge-pump PLL will be discussed in detail. Phase noise analysis using a small-signal model will be described and noise-bandwidth-power tradeoffs will be presented. Existing and emerging techniques to alleviate these tradeoffs will be briefly discussed.

Pavan Kumar Hanumolu received the Ph.D. degree in electrical engineering from Oregon State University in 2006. Currently, he is an Assistant Professor in the School of Electrical Engineering and Computer Science at the same University. Pavan received the NSF CAREER award and has served as the Associate Editor of IEEE Transaction Circuits and Systems and Guest Editor of the Journal of Solid-State Circuits. His research interests include high-speed I/O interfaces, digital techniques to compensate for analog circuit imperfections, time-based signal processing, and power-management circuits.

3:30 pm – 5:20 pm

### **E4-2 Spectral Purity Issues in Fractional-N Frequency Synthesis**

Sudhakar Pamarti, UCLA

This short course will introduce the basics of fractional-N based phase locked loops and discuss important performance concerns such as phase noise and spurious tones and means of addressing them.

Dr. Sudhakar Pamarti is an Associate Professor of Electrical Engineering at the University of California, Los Angeles. He received his PhD degree from the University of California, San Diego in 2003. Prior to joining UCLA in 2005, he worked at Rambus Inc. His current research interests are in integrated circuit design especially in using signal processing techniques to improve circuit performance.

## Educational Session Track 5 – Designing Smart Sensors in MEMS and CMOS

Fir Ballroom, Sunday, September 18

Organizer: Farrokh Ayazi, Georgia Institute of Technology  
Co-Organizer: Ada Poon, Stanford University

Sensors are everywhere! Temperature sensors throttle SoCs, accelerometers activate airbags, and gyroscopes and magnetometers are now standard smart phone components. These are all examples of smart sensors, i.e. sensors that are co-integrated with their readout electronics, are adaptable and reconfigurable, and provide digital output. However, processing the weak analog output of typical sensors is quite challenging, especially when it must be done in standard CMOS, whose precision is limited by  $1/f$  noise, component tolerances and mismatch. In this tutorial, a system approach to the design of smart sensors will be presented. The use of dynamic techniques, such as chopping, auto-zeroing, dynamic element matching and sigma-delta modulation, to trade speed for precision will be discussed. The proposed methodology will be illustrated by case studies describing the design of state-of-the-art sensors for the measurement of wind velocity, magnetic field, temperature, acceleration, angle of rotation, and mass.

1:30 pm - 3:20 pm

### **E5-1 CMOS-Based Sensors**

Kofi A.A. Makinwa, Delft University

Kofi A.A. Makinwa is a Professor at Delft University of Technology, The Netherlands, where he leads a group that designs precision analog circuits,  $\Sigma\Delta$  modulators, and smart sensors. He holds B.Sc. (1<sup>st</sup> Class Hons.) and M.Sc. degrees from Obafemi Awolowo University, Nigeria, an M.E.E. (*cum laude*) degree from the Philips International Institute, The Netherlands and a Ph.D. degree from Delft University of Technology. From 1989 to 1999 he was a research scientist at Philips Research Laboratories, after which he joined Delft University of Technology. He holds 14 patents, has (co)-authored 1 book and over 140 technical papers, and has given tutorials and invited talks at several international conferences, including the ISSCC. Dr. Makinwa is a recipient of the Dutch Technology Foundation's Simon Stevin Gezel award, and is a (co)-recipient of JSSC, ISSCC, ESSCIRC and Transducers best paper awards, among others. He is an IEEE fellow and distinguished lecturer as well as a member of the Young Academy of the Royal Netherlands Academy of Arts and Sciences.

3:30 pm – 5:20 pm

### **E5-2 MEMS-Based Sensors**

Farrokh Ayazi, Georgia Institute of Technology

Farrokh Ayazi is a Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, and a director of the Center for MEMS and Microsystems Technologies (CMMT) at Georgia Tech. He received the B.S. degree in electrical engineering from the University of Tehran, Iran, in 1994 and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1997 and 2000, respectively. His main research interest lies in the area of Integrated Micro-Electro-Mechanical Systems (Integrated

MEMS), focusing on resonators, inertial sensors, and mixed-signal interface circuits for MEMS and Sensors. Dr. Ayazi is an editor for the IEEE/ASME Journal of Micro-Electro-Mechanical Systems. He is a 2004 recipient of the NSF CAREER Award, the 2004 Richard M. Bass Outstanding Teacher Award (determined by the vote of the ECE senior class), and the Georgia Tech College of Engineering Cutting Edge Research Award for 2001–2002. He and his students won the best paper awards at Transducers 2011, the IEEE International Frequency Control Symposium in 2010, and IEEE Sensors conference in 2007.

Dr. Ayazi is the Co-Founder and Chief Technology Officer of Qualtré Inc., a spin-out from his research Laboratory that commercializes multi-axis Bulk Acoustic Wave (BAW) silicon gyroscopes and six-degrees-of-freedom inertial sensors for consumer electronics and personal navigation systems.

**Educational Session Track 6 – 3D ICs**

Pine Ballroom, Sunday, September 18

Organizer: Mike Li, Altera  
Co-Organizer: Vikas Chandra, ARM

1:30 pm - 3:20 pm

**E6-1 3D Technology – Status and Opportunities**

Pol Marchal, IMEC

In recent years, industry has spent significant efforts in developing 3D process technology. It enables interconnecting multiple stacked dies, possibly in made in different process technologies and originating from different fabs, at a >16x higher IO density than today's packaging solutions. TSVs and ubumps are the cornerstones of this technology for which process solutions, reliability and design rules are becoming available. In this talk, we will review status of 3D from both design and technology perspective, and based here on indicate likely system opportunities for 3D for both high performance systems as well as mobile devices.

Pol Marchal holds a position as principal scientist at IMEC. Currently, he is leading an initiative to set up a design center for products and solutions in emerging markets. Prior to this assignment, he initiated and led imec's 3D design initiative and insite program. He received the engineering degree and Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium in 1999 and 2005 respectively. He has a background that combines technology R&D with system and product development.

3:30 pm - 5:20 pm

**E6-2 3-D Integration: Materials, Technologies, Schemes, and Applications**

Chuan Seng Tan, National Technological University

Three-dimensional (3-D) integration of ultra-thin ICs is identified as an inevitable solution for future system miniaturization and functional diversification. In this 3-D implementation, thinned IC layers are seamlessly bonded with a reliable bonding medium and electrically interconnected with through silicon via (TSV). This talk provides an overview of the emerging field of 3-D integration of integrated circuits. It covers motivations and potential benefits, materials selection, technology platforms, and process integration strategies. Different 3-D integration schemes are discussed. Key technologies, including TSV, bonding, thinning and handling, are introduced. An updated status on application drivers will be given as well as a list of challenges faced by the industry. It ends with an outlook on future development in this exciting and promising field.

Chuan Seng Tan received his B.Eng. degree in electrical engineering from University of Malaya, Malaysia, in 1999. Subsequently, he completed his M.Eng. degree in advanced materials from the National University of Singapore under the Singapore-MIT Alliance (SMA) program in 2001. He then joined the Institute of Microelectronics, Singapore, as a research engineer where he worked on process integration of strained-Si/relaxed-SiGe heterostructure devices. In the fall of 2001, he began his doctoral work at the Massachusetts Institute of Technology, Cambridge, USA, and was awarded a Ph.D. degree in electrical engineering in 2006. He was the recipient of the Applied Materials Graduate Fellowship for 2003-2005. In 2003, he spent his summer interning at Intel Corporation, Oregon. He joined NTU in 2006 as a Lee Kuan Yew Postdoctoral Fellow and since July 2008, he is a holder of the inaugural Nanyang Assistant Professorship. His research interests are semiconductor process technology and device physics. Currently he is working on process technology of three-dimensional integrated circuits (3-D ICs). He co-edited a book on "Wafer Level 3-D ICs Process Technology" and it was published by Springer (ISBN 978-0-387-76532-7). A second edited volume entitled "3D Integration of VLSI Systems" will be published by Pan Stanford Publishing (ISBN 978-981-4303-81-1) in summer 2011. He has numerous publications on 3-D technology. He provides his service as committee member for International Conference on Wafer Bonding and IEEE International 3D System Integration Conference. He is a member of IEEE.