

EDUCATIONAL SESSIONS

Sunday, September 19

Chairperson: Ramesh Harjani, University of Minnesota

Educational Session Track 1 - Fundamentals

Synthesizers & PLLs

Oak Ballroom, Sunday, September 19

Organizer: Pavan Hanumolu, Oregon State University

Co-Organizer: Shahriar Mirabbassi, University of British Columbia

8:30 am - 10:20 am

E1-1 Phase-Locking Techniques for Frequency Synthesis

Pavan Hanumolu, Oregon State University

Phase-locked loops (PLLs) are essential building blocks in all digital, analog, and radio-frequency integrated circuits (ICs). The noise, power, and area of PLLs determine many of the key performance parameters in all such ICs. This tutorial describes the fundamental principles and concepts of PLL design. After reviewing the operation of a simple type-1 PLL and the characteristics of its building blocks, the operating and design principles of a charge-pump PLL will be discussed in detail. Phase noise analysis using a small-signal model will be described and noise-bandwidth-power tradeoffs will be presented. Existing and emerging techniques to alleviate these tradeoffs will be briefly discussed.

10:30 am - 12:20 pm

E1-2 Design Techniques for Analog PLLs: Moving Beyond Classical Topologies

Mike Perrot, SiTime Corporation

This lecture provides design techniques for advanced analog PLLs. It builds on the previous lecture by further explaining the key properties of the charge pump PLL that have made it so attractive as the topology of choice. Possible alternatives to achieve a less design intensive implementation while still obtaining the required performance will be examined. More advanced design possibilities such as high gain phase detectors, sampled and switched resistor loop filter topologies, and switched capacitor frequency acquisition circuits will be presented. The talk will conclude by showing results from a recent example that utilizes these concepts to achieve a low power and area PLL implementation targeted to a MEMS-based oscillator circuit.

1:30 pm - 3:20 pm

E1-3 Fractional-N PLLs

Ian Galton, University of California, San Diego

This lecture provides an explanation of the fractional-N PLL as an extension of the integer-N PLL. It builds on previous lectures by explaining the additional ideas and issues associated with fractional-N PLLs relative to integer-N PLLs. Topics include a self-contained overview of delta-sigma modulation, tradeoffs associated with quantization noise shaping order and PLL bandwidth, non-ideal effects of particular concern in fractional-N PLLs, spurious tone generation mechanisms and mitigation techniques, and recently developed techniques to enhance fractional-N PLL performance. Many of the concepts are presented in the context of fractional-N PLL CMOS IC case studies supported by measurement results.

3:30 pm – 5:20 pm

E1-4 All-Digital Phase Locked Loop: Successes and Challenges

Kurram Waheed, Freescale Semiconductor

Traditional PLL techniques using a charge-pump PLL require a design flow and circuit techniques, which are quite analog and area intensive. At times, high performance analog PLL designs utilize process technologies that are either incompatible with the bulk digital processor and memory circuits, or simply do not allow for aggressive area/power scaling as the process nodes continue to shrink. This tutorial explains

the design concepts of a digitally controlled oscillator (DCO)-based all-digital phase locked loop (ADPLL) architecture for frequency synthesis in wireless RF applications. Techniques to avoid analog tuning, to achieve fine frequency resolution, seamless integration of ripple cancellation, wider modulation bandwidths, faster settling time using gear-shifting, and compensation of analog-digital inter-conversion imperfections through digital signal processing means will be presented. The tutorial will conclude with a description of multiple generations of ADPLL architectures

Educational Session Track 2 – Advanced Topics

Wireless

Fir Ballroom, Sunday, September 19

Organizer: Howard Luong, HKUST

Co-Organizer: Ramesh Harjani, University of Minnesota

8:30 am – 10:20 am

E2-1 Highly Integrated and Tunable RF Front-Ends for SDRs

Hooman Darabi, Broadcom Corporation

RF front-end passives, such as SAW filters or duplexers, have proven resistant to integration as part of a low-cost CMOS system-on chip (SoC). Traditional RF designs are unsuitable because of the modest quality factor for on-chip spiral inductors as well as manufacturing variation of on-chip capacitors. Aside from higher cost and bigger physical space, the lack of any tunability in such external components prevents the use of highly reconfigurable transceiver front-ends for soft-ware defined or cognitive radio applications. In this tutorial, architectural and circuit techniques to integrate the RF front-end passive components, namely the SAW filters and duplexers that are traditionally implemented off-chip, are presented. We first study the system level requirements for front-end passives and discuss the SoC implementation challenges from the circuit point of view. We then introduce several architectural and circuit level techniques that can address these problems, followed by case studies for both 2G and 3G transceivers.

10:30 am – 12:20 pm

E2-2 Phased Arrays: Transceiver Architectures, Monolithic Implementations, and Applications

Hossien Hashemi, University of Southern California

The data-rate of wireless communication systems is limited by signal to noise plus interference (SNIR). Multiple antenna systems can improve the SNIR by dynamically focusing the transmit power towards the desired directions, reducing the interferences through spatial filtering, and improving the receiver sensitivity. Phased arrays have been around for over half a century in high performance military radar and communication systems. Recently, monolithic realization of these systems in silicon has enabled commercial applications such as reliable high-speed wireless communication at 60GHz, low-cost automotive radars at 24GHz and 77GHz, ultra wideband imaging systems at 3-18GHz, and millimeter-wave imaging for security and healthcare applications. This tutorial covers the basics of multi-antenna systems, narrowband phased arrays, wideband timed arrays, transceiver architectures, circuit building blocks, and several case studies spanning 1-100GHz for various applications.

Wireline

Fir Ballroom, Sunday, September 19

Organizer: Mike Li, Altera

Co-Organizer: Ken Chang, Rambus, Inc.

1:30 pm – 5:20 pm

E2-3 Energy Efficient I/O: Multi-Gb/s Link Design and Power Management Techniques

Brian Casper, Intel Circuit Research Laboratory and Tony Carusone, University of Toronto

This session looks at the major challenge facing computer and networking systems now and for the next decade: I/O energy efficiency. Aggregate I/O bandwidth must increase aggressively to take full advantage of tomorrow's highly parallel processors, but the total power available for I/O is constrained. No single strategy appears to offer the energy-efficiency improvements that will be required in the next decade. Rather, the entire system must be co-optimized including the channel, transmitter, receiver, and clocking circuits, with the objective function being energy consumption per communicated bit. This optimized system must then exploit a combination of power management techniques including burst-mode operation, low-power standby, dynamic voltage and frequency scaling, and dynamic link narrowing. In this session, we will look at the challenge and each of these solutions, using case studies to illustrate the current state-of-the-art. It will conclude with a look forward, speculating on research thrusts that are most likely to have an impact in this area over the next 5-10 years.

Educational Session Track 3 – Advanced Topics

Power Management

Pine Ballroom, Sunday, September 19

Organizer: Gordon Lee, Qualcomm

Co-Organizer: Cory Arnold, Maxim Integrated Products

8:30 am - 10:20 am

E3-1 Good Analog Approaches to Power Circuits and Systems

Robert Pease, NSC

Analog techniques are still applicable to good, high-performance power systems. Often system limitations involve thermal quantities and inductive coupling which are nonlinear, hard to quantify, and not subject to computerized analysis or optimization. This is true for discrete power circuits, and systems in silicon. Not to mention high-power systems in other worlds. In other words, you have to THINK. In other words, you have to BUILD IT to be sure it works. Many examples will be discussed along with intuition, insights, physical relationships, 3-dimensional flows, symmetry, and more...examples will be fun!

10:30 am - 12:20 am

E3-2 Smart Power Management Using Digitally Controlled Switched-Mode Power Converters

Dragan Maksimovic, University of Colorado

Effective and efficient power management is critically important in a very wide range of electronic systems, such as micro-power energy harvesting devices, battery-powered portable devices, desktop computers, computing and telecommunication infrastructure, as well as renewable energy sources. The seminar starts by identifying power management challenges system examples, and points to solutions based on smart, digitally controlled switched-mode power converters. Approaches to practical realizations of high-frequency digital PWM controller integrated circuits are then reviewed, followed by presentations of dynamic performance and on-line efficiency improvement techniques. The seminar concludes with examples of system power management applications of digitally controlled switched-mode power converters in portable devices, high-efficiency off-line power adapters, and data server power systems

ADCs

Pine Ballroom, Sunday, September 19

Organizer: George LaRue, Washington State University

Co-Organizer: Sang-Soo Lee, Hynix Semiconductor America

1:30 pm - 3:20 pm

E3-3 Ghz ADCs: From Exotic to Mainstream

Ken Poulton, Agilent Research Laboratories and Mike Flynn, University of Michigan

Advances in CMOS technology and new circuit techniques have enabled GHz rate analog to digital conversion with good energy efficiency. The performance of low-resolution flash ADCs is closely tied to process technology, and nanometer technologies permit very high sampling rates. Folding has been employed to achieve higher resolution at these rates. Interleaved successive-approximation converters achieve very high sampling rates and excellent energy efficiency. These techniques as well as factors that limit ADC performance will be reviewed in part 1 of this tutorial. The progression of the fastest ADCs in the world, until recently the domain of oscilloscope ADCs, has now been invaded by communications-focused designs. In part 2 of the tutorial, the succession of technologies and architectures used will be described, from GaAs FETs to bipolar to today's CMOS.

3:30 pm - 5:20 pm

E3-4 Design Techniques for High-Performance Continuous-Time Delta-Sigma ADCs

Shanti Pavan Yendluri, Indian Institute of Technology-Madras

Continuous-time oversampling converters are becoming increasingly important in signal processing chains. In this tutorial, we examine several common problems encountered in their design, with a new perspective. We address the systematic design of such converters accounting for practical opamp nonidealities, DAC pulse shapes, and excess loop delay. We then give intuition for the effect of opamp nonlinearity in CT-sigma delta converters, and present techniques for rapidly simulating these effects. Further, opamp and circuit design techniques that enhance linearity will be discussed, with appropriate practical examples and case studies.