

**IEEE**

Custom Integrated Circuits Conference

**CICC 2008 CALL FOR PAPERS**

CICC showcases first-published innovative analog and digital circuit techniques covering a broad spectrum of technical topics.



**September 21 - 24, 2008**  
**San Jose, CA USA**  
**DoubleTree Hotel**

**Paper Submission Deadline:**  
**April 7, 2008**  
 For author instructions and electronic submission visit our web site at <http://www.ieee-cicc.org>

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**Conference Coordinator:** Melissa Widerkehr, Wderkehr & Assoc., [cicc@his.com](mailto:cicc@his.com)

**Analog Design:** amplifiers, filters, converters...

**Biomedical, Sensors, Displays, and MEMS:** biomedical, imaging, carbon nanotubes, displays...

**Digital and Mixed Signal SOC/ASIC/SIP:** solutions to today's complex digital and mixed-signal design problems...

**Embedded Memory:** scalability, GHz speed, low leakage...

**Manufacturing:** advanced processing and packaging, design impact of process-technology selection...

**Power Management:** AC/DC, DC/DC converters, regulators, regulator control, and power scavenging circuits...

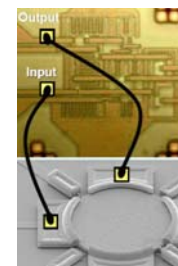
**Programmable Devices:** FPGAs, programmable I/Os...

**Simulation and Modeling:** Analog, RF, mixed-signal...

**Test, Characterization, Debug, and Reliability:** Design for test, RF characterization, at-speed test, reliability and failure analysis,....

**Wireless Designs:** circuits for cellular, connectivity, broadband, ultra low power, digital consumer broadcasting, diversity based systems, software defined radio....

**Wired Communications:** high speed electrical and optical, LAN, WAN, Ethernet, SONET, SerDes, modems, broadband, PLLs, DLLs...



**Technical Education** on new, state-of-the-art developments is the core of CICC. Over 160 papers, addressing a broad range of circuits, applications, design techniques, tools, test, reliability, and system-on-a-chip. Awards for Best Paper will be given for regular, invited, student, and poster submission categories. Top-rated CICC papers are eligible to be considered for the IEEE Journal of Solid State Circuits.

**Educational Sessions (September 21):** three in-depth, full-day tutorials instructed by recognized invited speakers.

- Fundamentals of Analog Design
- High-Speed Serial I/O
- Coping with Technology Scaling

**An opening Keynote address, Exhibits, interactive Poster-papers and Demonstrations, lively and controversial Panel Discussions, and a Luncheon** with guest speaker rounds out the program.

**The DoubleTree Hotel Conference Center** is minutes from SJC airport. San Jose offers easy access to many California destinations such as San Francisco, the Monterey peninsula on the Pacific, Wine Country, and Yosemite National Park.

IEEE CUSTOM INTEGRATED CIRCUITS CONFERENCE

*"Showcase for Circuit Design in the heart of Silicon Valley"*[www.ieee-cicc.org](http://www.ieee-cicc.org)

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## CICC is soliciting papers in the following areas

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**Analog Circuit Design:** Amplifiers, voltage references and regulators, opamps, sample-and-hold circuits, continuous and discrete-time filters, oversampled and Nyquist-rate data converters, non-linear analog circuits, mixed analog/digital IC applications, analog circuits for sensor interfaces, low-voltage/low-power analog, and deep submicron issues in analog design.

**Biomedical, Sensors, Displays, and MEMS:** Emerging technologies for sensors, displays, MEMS, and biomedical applications including materials, and methodologies. Examples include nanotechnology, microchemical sensors, biosensors and devices, image sensors, OLED's, DNA microarrays, carbon nanotubes, micro- and nanofluidic chips, novel display technologies and plastic circuitry. Alternative techniques for energy scavenging using photovoltaic and electrochemical sources.

**Digital and Mixed Signal SOC/ASIC/SIP:** Solutions to today's complex digital and mixed-signal design problems, in particular practical examples and case studies involved with system level design using SoC/ASICs/SiPs ("how we did it"). Digitizing analog functions that are difficult to design as technology processes scale. Interfacing analog and digital in the same chip including testing. Issues with large digital designs including power management, clocking and what to do when synthesis breaks. Examples of using SIP for a system solution.

**Embedded Memory:** Memory circuits, architectures, and methodologies addressing scalability, GHz performance, manufacturability, reliability, and the advancement of emerging memory technologies. Also of interest are redundancy, BIST, SER, cell stability, and low voltage/leakage design.

**Manufacturing:** Special focus on challenges of and alternatives to CMOS scaling, Design for Manufacturability, cost-effective manufacturing techniques, design impact of process-technology selection or packaging. Advanced manufacturing techniques using any combination of bulk/SOI CMOS, bipolar, non-silicon, and optoelectronics technologies. Evolving chip packaging such as chip stacking, lead-free, flip-chip, and System-in-Package. Tutorial papers are encouraged.

**Power Management:** Analog and digital circuit design for limiting integrated circuit power dissipation and power management. Circuits and architectures to limit active and standby power dissipation in digital circuits and memories. Advanced low power AC/DC, DC/DC converters, regulators, regulator control, and IO circuits. Integrated circuits implementing energy scavenging and power harvesting techniques. Systems implementing wireless power transmission, e.g., biomedical implants.

**Programmable Devices:** Logic block, routing fabric, system architecture, and circuit design for FPGAs, PLDs, and structured arrays. Programmable I/O structures, configurable cores, interaction between configurable logic and processors/memories/fixed-function cores. Programmable analog architectures. CAD tools targeting these devices. Power efficient architecture, power modeling and optimization for programmable devices. Architecture and CAD for nano-scale FPGAs.

**Simulation and Modeling:** Compact active and passive device models, behavioral modeling, and signal integrity modeling and simulation. Parasitic extraction and reduction. Simulation techniques for analog, RF, and mixed-signal circuits. Package modeling. Process variation, statistical, and reliability modeling. Compact models for extreme environment operation. SOI and multiple gate device modeling.

**Test, Characterization, Debug, and Reliability:** Design for test/manufacturability/reliability, built-in-self-test for IC system and low cost test techniques, design for at speed test, RF characterization and production test, jitter characterization and manufacturing test for high speed SerDes, hardware and firmware IC debug and diagnosis, new reliability and failure mechanisms in nanometer technologies, ESD protection, latch-up and soft errors. Tutorial papers in the areas of debug and diagnosis, and high speed serial I/O testing are encouraged.

**Wired Communications:** Circuits and systems for electrical and optical networks, including; peripheral IO buses, LAN, WAN, Ethernet, SONET, xDSL, SATA, HDMI, PCIe, USB, cable modems, power-line/phone-line home networks, serial links, backplane, high-speed memory and graphic interfaces, chip-to-chip interconnects, clocking and high-speed low-power blocks for broadband applications. Circuit blocks including Gbps-ESD, Serializers/Deserializers, Equalizers, PLLs, DLLs, CDRs, Oscillators, Drivers and Amplifiers.

**Wireless Designs:** Integrated wireless transceiver architectures and sub-circuits for cellular, connectivity, broadband and millimeter-wave communication, low-power and biomedical, smart antennas and MIMO, software-defined radio. Papers on RF circuit solutions targeting emerging wireless applications and techniques are particularly encouraged.

## Submission of Papers

*Paper Submission Deadline is April 7, 2008*

Papers must report original and previously unpublished work, including specific results. Papers may be up to 4 pages in length including illustrations, charts, tables and references. Successful submissions concisely explain how the work advances the state of the art and include schematics, measured results, and sufficient detail to convey key concepts. **Circuit-design papers intended for traditional lecture presentation must include measured experimental results that substantiate performance claims.** Circuit-design papers using only simulation to substantiate performance claims are usually rejected for traditional lecture presentation, but may be considered for poster presentation.

Papers are submitted electronically. **Prior** to preparing your paper for electronic submission, please read the paper preparation and submission guidelines on the CICC website ([www.ieee-cicc.org](http://www.ieee-cicc.org)). The submission instructions will be available by February 15. The submission page will be active beginning March 10.

When submitting a paper, please indicate a preference for **traditional lecture** or **poster presentation**, although CICC may assign presentations to either category.

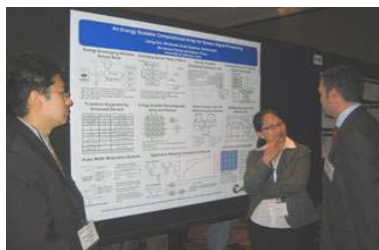
Appropriate company and government clearances **MUST** be obtained prior to submission. **IF A SIGNED COPYRIGHT FORM IS NOT RECEIVED WITH THE SUBMISSION, THE SUBMISSION WILL NOT BE REVIEWED.** Authors of accepted papers will be notified by email by June 9, 2008.

ACCEPTED PAPERS WILL BE PRINTED IN THE PROCEEDINGS WITHOUT OPPORTUNITY FOR FURTHER CHANGE.

Accepted papers will be used for publicity purposes and portions of these papers may be quoted in pre-conference magazine articles and also via the Web. If this is not acceptable, authors must email CICC at [cicc@his.com](mailto:cicc@his.com) to decline publicity.

### **Papers for Poster Presentation**

Poster presentations encourage in-depth discussions with the audience and are ideal for the presentation of ongoing research. The Poster Sessions are held during the conference receptions and exhibits, providing an exciting atmosphere and lively discussions between authors and attendees. The acceptance criteria for papers for poster presentation are identical to those for traditional lecture presentation except that the requirement for measured experimental results may be relaxed for papers intended for poster presentation.

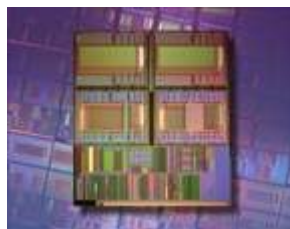


### **Tutorial Papers**

Tutorial papers may be up to 8 pages. Those interested in submitting a tutorial paper must contact the Technical Program Chair, Jackie Snyder ([jacqueline.snyder@marvell.com](mailto:jacqueline.snyder@marvell.com)) in advance. This should be as soon as possible, as the number of tutorial slots is limited.

### **Poster Session Demonstrations**

Lecture or poster presenters may apply to present a demonstration of their research. Visit the CICC website for additional details.



For complete instructions on submitting a paper, registration information and general inquiries:

**Visit our web site at [www.ieee-cicc.org](http://www.ieee-cicc.org)**

Or you can contact the Conference Office: IEEE Custom Integrated Circuits Conference, 19803 Laurel Valley Place, Montgomery Village, MD, 20886, Telephone: 301/527-0900 x101, Fax: 301/527-0994, email: [cicc@his.com](mailto:cicc@his.com),

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The IEEE Custom Integrated Circuits Conference is sponsored by:



The Institute of  
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Engineers, Inc.



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