

**REGULAR**  
**PAPER PREPARATION KIT FOR THE**  
**CUSTOM INTEGRATED CIRCUITS CONFERENCE**  
May 6- 9, 2001, Town and County Hotel, San Diego, CA

Dear Author(s):

We appreciate your interest in submitting a paper to the Custom Integrated Circuits Conference, May 6 - 9, 2001, in San Diego, CA. The Conference is following a policy of reviewing the complete camera-ready papers instead of preliminary abstracts. **The accepted papers will be printed in the CICC Conference Proceedings and CD ROM as submitted, without opportunity for further changes.** Enclosed in this Paper Preparation Kit you will find all the necessary information and forms for the preparation of your submitted paper.

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In order to insure that your submitted paper receives a complete review it is imperative that you follow all the instructions and submit all the required documentation. Enclosed to assist you are:

1. GENERAL GUIDELINES that address the deadlines and required documentation
2. AUTHOR'S GUIDE that provides a detailed description of camera-ready paper preparation
3. TECHNICAL CATEGORIES for paper submission
4. SAMPLE OF A COMPLETED PAGE
5. COPYRIGHT RELEASE FORM giving the conference permission to print the paper if accepted

**The deadline for submission of camera-ready papers is November 29, 2000.** Your cover letter, camera-ready paper (**plus 25 copies**), 50 word abstract, PDF copy of the paper on a floppy disk and copyright release form **NEED TO ARRIVE** at the Conference Office by that date. PLEASE REMEMBER THAT YOUR COMPLETED PAPER MUST OCCUPY NO MORE THAN FOUR PAGES (or 1.44MB).

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Phil Diodato  
Technical Program Chairman  
Custom Integrated Circuit Conference

Enclosures

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# AUTHOR'S GUIDE

## Preparation of Papers in Two-Column Format for the CICC

Center the Authors Names Here

Center the Affiliations Here

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(it is your option if you want your entire address listed)

### Abstract

The abstract is a brief (50 - 80 word) synopsis of your paper. It's use is to provide a quick outline of your presentation, giving the reader an overview of the research. This is an important aspect of your paper as it is this description that may attract the reader to continue and finish reading your full report.

### Introduction

These instructions give you basic guidelines for preparing camera-ready (CR) papers for the CICC. The instructions assume that you have computer desktop publishing equipment with several fonts. If you do not, and will be using a typewriter to prepare your paper, use 75% reduction mats (contact the CICC for mats).

Your goal is to simulate, as closely as possible, the usual appearance of published papers in the CICC Conference Proceedings. These instructions have been prepared in the preferred format.

### How to Format the Page

#### A. Full-Size Camera-Ready (CR) Copy

Prepare your CR paper in full-size format, on paper 8 1/2" x 11" (21.5cm x 27.9cm). If you are using A4 (metric) size paper, please cut the paper length to 28cm before you print the text.

#### B. Fonts

The best results will be obtained if your computer word-processor has several font sizes. Try to follow the font sizes specified in Table I as best you can. As an aid to gauging font size, 1 point is about 0.35mm. Use a proportional, serif font such as Times or Dutch Roman.

TABLE I  
FONT SIZES FOR CAMERA-READY PAPERS

Font Size	Bold	Italic	Text
10			Main Text, Authors Affiliations
10	Yes		Headings, i.e., <b>Abstract</b>
12			Authors' names
14	Yes		Paper title
10		Yes	Subheadings, i.e., <i>Fonts</i>
8			Section titles, references, tables table names, table captions, figure captions, footnotes, sub-and superscripts

### C. Format

In formatting your paper, set top and bottom margins to 1 inch (25mm) and left and right margins to 0.70 inches (19mm). If you are using A4 paper, set the right margin to 12mm. The column width is 3.45 inches (88mm) with 0.2 inches (5mm) space between the two columns.

You should left- and right-justify your columns. On the last page of your paper, try to adjust the lengths of the two columns so that they are the same. Use automatic hyphenation if you have it. Don't forget to check spelling.

Single space between a heading and the following text. Double space between text and the following heading.

**Number each of your submitted pages at the top, right corner, in non-photographic light blue pencil.**

### D. Reduction Mats

If you have only typewriter fonts available, use 75% reduction mats (model paper). **Contact the CICC Office immediately (telephone: 301/527-0900, fax: 301/527-0994) and mats will be sent to you.**

### Illustrations

Position figures and tables at the tops and bottoms of columns if possible. Large figures and tables may span both columns. Figure captions should be below the figures; table captions should be above the tables. Try to place the figures and tables after their first mention in the text. Use the abbreviation (e.g., "Fig. 1") even at the beginning of a sentence.

All halftone illustrations (pictures/photographs) should be clear black and white prints. Do not use photocopies. These illustrations should be furnished within the copy, or if necessary, as separate 8" x 10" prints, in which case a blank space of proper proportions must be allowed within the copy. Halftone illustrations not so designated will be placed at the end of the respective paper. Make certain to include a caption in the paper for the illustration as well as to label the illustration on the back.

### Helpful Hints

#### A. References

List and number all references at the end of the paper. When referring to them in the text, type the corresponding reference number in parentheses as shown at the end of this sentence (1). Number the citations consecutively. The sentence punctuation follows the parentheses. Do not use "Ref. (3)" or "reference (3)" except at the beginning of a sentence.

Number the footnotes separately in superscripts<sup>1</sup>. Place the actual footnote at the bottom of the column in which it is cited. Do not put footnotes in the reference list.

Give all authors' names; do not use "et al" unless there are six authors or more. Papers that have not been published, even if they have been submitted for publication, should be cited as "unpublished" (10). Papers that have been accepted for publication should be cited as "in press" (11). Capitalize only the first word in a paper title, except for proper nouns and element symbols.

For papers published in translation journals, please give the English citation first, followed by the original foreign-language citations (12).

#### *B. Abbreviations and Acronyms*

Define abbreviations and acronyms the first time they are used. Acronyms such as MOSFET, ac and dc do not have to be defined. Define acronyms when first used in the text even if they have been defined subsequently in the paper.

#### *C. Equations*

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). To make your equations more complex, you may use the solidus (/), the exp function, or appropriate exponents. Italicize Roman symbols for quantities and variables, but not Greek symbols. Use a long dash rather than a hyphen for a minus sign. Use parentheses to avoid ambiguities in denominators. Punctuate equations with commas or periods when they are part of a sentence.

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. When you refer to equations in the text, refer to (1). Do not use "Eq. (1)" or "Equation (1)" except at the beginning of a sentence: Equation (1) is used...

#### *D. Other Recommendations*

Use either one or two spaces between sections, and between text and tables or figures, to manipulate the column length. Use two spaces after periods at the end of sentences (full stops).

### **References**

- (1) G. Eason, B. Noble, and I.N. Sneddon, "On certain integrals of Lipschitz-Hankel type involving products of Bessel functions," *Phil. Trans. Roy. Soc. London*, vol. A247, pp. 529-551, April 1955.
- (2) J. Clerk Maxwell, *A Treatise on Electricity and Magnetism*, 3rd ed., Vol. 2, Oxford: Clarendon Press, 1892, pp. 68-73.
- (3) I.S. Jacobs and C.P. Bean, "Fine particles, thin films and exchange anisotropy," in *Magnetism*, Vol. III, G. T. Rado and H. Suhl, Eds., New York: Academic Press, 1963, pp. 271-350.
- (10) M. Smith, "Title of paper optional here," unpublished.
- (11) K. Rose, "Title of paper with only first word capitalized," in press.
- (12) Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," *IEEE Trans. J. Magn. Japan*, vol. 2, pp. 740-741, August 1987 [*Digests 9th Annual conf. Magn. Japan*, p. 3012, 1982]

## TECHNICAL CATEGORIES

### PAPERS IN THE FOLLOWING AREAS ARE REQUESTED:

<p><b>Communications</b> Analog, Wired and Wireless Circuits</p>	<p>Data converters, modulators, filters, high-speed analog, low voltage techniques. Mixed analog-digital IC applications, disk read/write channels, RAMDACs.</p> <p>Data, voice, image and video transmission. Digital, analog modulation, equalization, error correction, coding, switching. SONET/SDH, xDSL, LAN/WAN/ATM, set-top receiver, cable modem, high-speed serial links and broadband applications. Advanced read-write channel ICs.</p> <p>Analog or mixed-signal integrated circuits and systems for voice and data communications. Receivers, transmitters, and their functional blocks. Mixed-signal innovations for auto calibration, adaptive signal processing, modulation and demodulation.</p>
<p><b>Digital Systems:</b> Embedded Memories, SOC, IP Generation and Project Management</p>	<p>Use of SRAM, DRAM, EPROM, EEPROM, ROM and CAM in ICs. Innovative memory architectures, sense amplifiers, special memory interfaces, low-power design techniques, and design of memories in new technologies such as SOI or ferroelectric material.</p> <p>System-on Chip (SoC) design, demonstration of IP usage, coverage of complete design flow. Complexity demonstrated in both gate count as well as type of functions integrated onto the same IC.</p> <p>IP generation, methodology implementation, use within conventional CAD flows, evaluation, and protection. IC design technical project management, design effort estimation, automation support resource estimation, multi-team design efforts, enterprise (24/7) design methodology.</p>
<p><b>Simulation-Modeling</b></p>	<p>Circuit, functional, timing, and logic simulation. Device and block modeling. Analog, RF modeling and simulation. Mixed signal simulation and modeling of analog/digital interfaces. Signal Integrity and Reliability Verification. Clock/Power Network design, synthesis and verification. R(L)C extraction and analysis. Modeling of device/interconnect process and variations.</p>
<p><b>DSP</b></p>	<p>Digital video and audio, MPEG, image recognition and enhancement. Audio coding and speech recognition. Specialized processing function architectures. Digital filtering, encryption, HDTV, video conferencing, multimedia, graphics controllers, video drivers, and novel DSP algorithm implementations.</p>
<p><b>Custom /Low-Power</b></p>	<p>Papers detailing custom circuit designs including low power and low voltage design techniques are requested. Innovative designs for cell based or full custom ICs for applications such as automotive, biomedical, and consumer. Sensor interface circuits and high-performance circuit designs, including dynamic logic, clocking circuits, and I/O circuits.</p>
<p><b>Programmable Devices</b></p>	<p>Innovations in EPLD, FPGA, PLD, PAL, GA device architecture and product features. Advances in circuit techniques, device and/or product feature applications, and CAD tools targeting these devices.</p>
<p><b>Fabrication / Foundry</b> Process, Foundry</p>	<p>Advanced process integration techniques for the manufacturing &amp; prototyping of system-on-a-chip ICs using any combination of CMOS, bipolar, SOI, BiCMOS, smart power, Ferroelectrics, and MEMS technologies. New and evolving chip packaging like BGA, flipchip, chip-on-chip, and multi-chip modules. Package modeling, techniques, ESD protection, and fiber optic transceivers.</p>
<p><b>Test and Reliability</b></p>	<p>Advances in design-for-testability (DFT), including analog design for test, fault modeling and grading, IDDQ measurements, scan, Analog and Digital BIST, and JTAG, parametric characterization, high speed or high frequency measurement techniques and failure analysis.</p>

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