

Monday Morning				
Time	Session 2 Advanced RF Circuit Simulation and Modeling	Session 3 IP Creation and Protection	Session 4 IC Design Project Management	Session 5 Audio and Video Signal Processing
10:00	Introduction	Introduction	Introduction	Introduction
Mon. 10:05	2.1 - Simulation and Modeling of Intermodulation Distortion in Communication Circuits, J. Chen et al., Cadence	3.1 - A Fully Synthesizable Parameterized Viterbi Decoder, R. Burger et al., STMicroelect. / CSELT, Italy	4.1 - Multi-Project Management in Real Time, K. Au, Motorola / T. Mann, AMS Inc., Redlands, CA	5.1 - A Scalable Architecture for MPEG-4 Embedded Zero Tree Coding, B. Vanhoof, et al., IMEC/DESICS, Heverlee, Belgium
Mon. 10:30	2.2 - Intermodulation Analysis of Mixer Circuits Based on Frequency Domain Relaxation Method, A. Ushida et al., Tokushima U., Sony	3.2 - Fast and Accurate Power Verification of a Viterbi Decoder IP based on Mixed-Level Power Simulation Technique with Automatic Spatio-Temporal Circuit Partitioning, M. Chinosi et al., STMicroelect., Italy		5.2 - A MPEG4 Programmable Codec DSP with an Embedded Pre/Post-Processing Engine, S. Kuromaru et al., Matsushita
Mon. 10:55	2.3 - Grid Selection Strategies for Time-Mapped Harmonic Balance Simulation of Circuits with Rapid Transitions, O. Nastov, Motorola / J. White, MIT	3.3 - Watermarking-Based Copyright Protection of Sequential Functions, I. Torunoglu, E. Charbon, Cadence	4.2 - Integrated IC Design Approach based on Software Engineering Paradigm, S. Sinha et al., TI, Bangalore, India	5.3 - A Low-Power Single-Chip MPEG-2 CODEC LSI, Y. Tsuboi et al., Hitachi
Mon. 11:20	2.4 - Automated Macromodelling of "Nonlinear" Wireless Blocks, J. Roychowdhury, Bell Labs	3.4 - Hierarchical Watermarking for Protection of DSP Filter Cores, A. Rashid et al., UCLA	4.3 - Beyond 1 GHz, H. Hofstee, K. Nowka, IBM, Austin	5.4 - Embedding DRAM in Single chip MPEG1 CODEC LSI, T. Fujihira et al., Hitachi

Mon. 11:45	2.5 - A Frequency-Domain, Volterra Series-Based Behavioral Simulation Tool for RF Systems, I. Vassiliou et al., UC Berkeley			
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Monday Afternoon				
Time	Session 6 System-On-Chip: Trends and Real Life Applications	Session 7 Data Converters	Session 8 IC Test and Reliability	Session 9 Programmable Logic Architectures
Mon. 2:00	Introduction	Introduction	Introduction	Introduction
Mon. 2:05	6.1 - The Changing Landscape of System-on-a-Chip Design (invited), A. Rincon et al., IBM, Essex Junction, VT	7.1 - CMOS Pipelined ADC Employing Dither to Improve Linearity, H. Fetterman et al., Bell Labs Lucent	8.1 - A Low-Triggering Circuitry for Dual-Direction ESD Protection, A. Wang et al., Illinois Inst. Tech. / National	9.1 - Simplifying In-System Programming: Evolving Standards for ISP (invited), B. Moyer, Altera
Mon. 2:30		7.2 - A 55-mW, 10-bit, 40Msamples/Nyquist Rate CMOS ADC, I. Mehr et al., Analog Devices	8.2 - New Experimental Methodology to Extract Compact Layout Rules for Latchup Prevention in Bulk CMOS ICs, M-D. Ker et al., Indust. Tech. Res. Inst. / Nat. Chiao-Tung Univ., Taiwan	
Mon. 2:55	6.2 - Intellectual Property Re-use and System Emulation the Keys to succeed the SOC Challenge: A Digital TV Application, G. Bollano et al., CSELT, Italy	7.3 - An 8-Bit 150-MHz CMOS A/D Converter, Y-T. Wang, B. Razavi, UCLA	8.3 - Test Chips for Die Stress Characterization using Arrays of CMOS Sensors, A. Bradley et al., Auburn Univ.	9.2 - Circuit Design, Transistor Sizing and Wire Layout of FPGA Interconnect, V. Betz et al., Univ. of Toronto

Mon. 3:20	6.3 - A Single-Chip MPEG2 422@ML Video, Audio, and System Encoder with a 162-MHz Media-Processor and Dual Motion Estimation Cores, S. Kumaki et al., Mitsubishi	7.4 - A 3.3V Single-Poly CMOS Audio ADC Delta-Sigma Modulator with 98dB Peak SINAD, E. Fogleman et al., UC San Diego	8.4 - Digital Detection of Parametric Faults in Data Converters, B. Vinnakota et al., Univ. of Minnesota	9.3 - A Next Generation Architecture Optimized for High Density System Level Integration, R. Cliff et al., Altera
Mon. 3:45	6.4 - An Analog Record, Playback and Processing System on a Chip for Mobile Communications Devices, G. Jackson et al., ISD Inc., San Jose, CA	7.5 - A Spurious-Free Delta-Sigma DAC using Rotated Data Weighted Averaging, R. Radke et al., LSI Logic / Wash. St. U.	8.5 - Testing Analog Circuits by Supply Voltage Variation and Supply Current Monitoring, Y. Kilic et al., Univ. of Southampton, UK	9.4 - A Fast, Predictable FPGA with PLLs, Dual Port SRAMs and Active Repeaters, P. Sasaki et al., DynaChip, Sunnyvale, CA
Mon. 4:10	6.5 - Single GSM Mixed Signal Superchip with 96K Bytes FLASH and Low Power Micro-Controller, K. Lee et al., Bell Labs Lucent	7.6 - A Bandpass Sigma-Delta Modulator IC with Digital Branch-Mismatch Correction, V. Comino, Lucent / A. Lu, HP Labs	8.6 - TRANSPARENT: A System for RTL Testability Analysis, DFT Guidance and Hierarchical Test Generation, Y. Makris et al., UC San Diego / Intel, Hillsboro, OR	9.5 - A Field Programmable System Chip which Combines FPGA and ASIC Circuitry, W. Andrew et al., Lucent
Mon. 4:35		7.7 - A 2.7V 11.8 mW Baseband ADC with 72 dB Dynamic Range for GSM Applications, A. Nagari et al., STMicroelect., Italy		9.6 - A 4.9ns, 3.3 Volt, 512 Macrocell, CMOS PLD with Hot Socket Protection and Fast In System Programming, B. Vest et al., Altera

Mon. 5:00				9.7 - Flexible Reconfigurable Multiplier Blocks Suitable for Enhancing the Architecture of FPGAs, S. Haynes et al., Imperial College, London / University de Aveiro, Portugal
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Tuesday Morning				
Time	Session 10 Wireless Transceivers and Systems	Session 11 Embedded Memory Circuits and Techniques	Session 12 LAN/WAN Transceiver Technology	Session 13 Custom Circuit Techniques for High-Performance and Low-Power Applications
Mon. 2:00	Introduction	Introduction	Introduction	Introduction
Tues. 8:30	Introduction	Introduction	Introduction	Introduction
Tues. 8:35	10.1 - RF Transmitter Architectures and Circuits (invited), B. Razavi, UCLA	11.1 - Converting a SRAM From Bulk Si to Partially Depleted SOI, M. Wood et al., IBM, Poughkeepsie, NY	12.1 - A CMOS Mixed-Signal 100Mb/s Receive Architecture for Fast Ethernet, A. Shoval et al., Lucent	13.1 - Design Considerations for Distributed Microsensor Systems (invited), A. Chandrakasan et al., MIT
Tues. 9:00		11.2 - Multiple Twisted Data Line Techniques for Coupling Noise Reduction in Embedded DRAMs, D-S. Min et al., Univ. of Pittsburgh	12.2 - A Dual-Speed 125Mbaud/10Mbaud CMOS Transmitter for Fast Ethernet, O. Shoaei et al., Lucent	
Tues. 9:25	10.2 - A 4-dB NF GPS Receiver Front-end with AGC and 2-b A/D, M. Cloutier et al., Philips, Ottawa	11.3 - A 1.8V, 2.0ns Cycle, 32KB Embedded Memory with Interleaved Castout/Reload, S. Sullivan et al., Motorola Somerset, Austin, TX	12.3 - Clock and Data Recovery for 1.25 Gb/s Ethernet Transceiver in 0.35um CMOS, K. Iravani et al., VLSI Tech., San Jose, CA	13.2 - A Single Chip CMOS APS Camera with Direct Frame Difference Output, S-Y. Ma, L-G. Chen, Nat. Taiwan Univ.

Tues. 9:50	10.3 - Mixed-Signal Quadrature Demodulator with a Multi-Carrier Regeneration Systems, J. van Lammeren et al., Philips, The Netherlands	11.4 - A Self-Timed, Fully-Parallel Content Addressable Queue for Switching Applications, J. Podaima et al., Univ. of Toronto	12.4 - A 1.25GHz 0.35um Monolithic CMOS PLL Clock Generator for Data Communications, L. Sun, T. Kwasniewski, Carleton Univ., Ottawa	13.3 - Band Runlength Coding for Low-Power Continuous Micro Monitors, M. Fujishima et al., Univ. of Tokyo
Tues. 10:15	10.4 - An Ultralow Power Single-Chip 900 MHz CMOS Receiver for Wireless Paging, H. Darabi, A. Abidi, UCLA	11.5 - A 1.4V 60MHz Access, 0.25um Embedded Flash EEPROM, T. Kataoka et al., Matsushita	12.5 - A 3V-CMOS Low Distortion Class AB Line Driver Suitable for HDSL Applications, M. Kappes, Conexant, San Diego, CA	13.4 - A Data-driven Micropipeline Structure using DSDCVSL, S. Mathew et al., SUNY, Buffalo, NY
Tues. 10:40	10.5 - A 5.2 GHz 3.3V I/Q SiGe RF Transceiver, J.-O. Plouchart et al., IBM, Yorktown Heights, NY	11.6 - Analog Sense Amplifiers for High Density NOR Flash Memories, M. Pasotti et al., STMicroelect., Italy	12.6 - A 2.5-GB/s One-Chip Receiver Module for Gigabit-To-The Home (GTTH) System, M. Soda et al., NEC	13.5 - A 62.5 - 250 MHz Multi-Phase Delay-Locked Loop Using a Replica Delay Line with Triply Controlled Delay Cells, Y. Moon et al., Seoul Nat. Univ. / Silicon Image, Cupertino, CA
Tues. 11:05	10.6 - A Si/SiGe HBT Timing Generator IC for High-Bandwidth Impulse Radio Applications, D. Rowe et al., Sierra Monolithics / Time Domain Systems / UC San Diego			13.6 - A +/-25ps Jitter 1.9v CMOS PLL for UltraSPARC Microprocessor, H-T. Ahn, Sun, Palo Alto, CA
Tuesday Afternoon				
Time	Session 14 Read/Write Channel Signal Processing	Session 15 Advanced Technologies for SOC and RF ICs	Session 16 Noise Modeling and Simulation In Communications Circuits	Session 17 IP Reuse and Infrastructure
Tues. 2:00	Introduction	Introduction	Introduction	Introduction

Tues. 4:10	14.5 - A BiCMOS Pre-amplifier/Write-driver IC for Tape Drive, M. Flynn et al., Silicon Systems Ltd., Cork, Ireland	15.4 - Pre-Silicon Parameter Generation Methodology using BSIM3 for Device/Circuit Concurrent Design, M. Miyama et al., Hitachi	16.5 - Modeling and Simulation of Noise in Analog/Mixed-Signal Communication Systems (invited), A. Demir et al., Bell Labs	17.5 - IP Repository, A Web based IP Reuse Infrastructure, P. Schindler et al., Motorola, Munich, Germany
Tues. 4:35	14.6 - A BiCMOS 1X to 5X Combined Analog Frontend IC for DVD-ROM & Movie Players, S. Marchese et al., STMicrolect., Italy / Thomson, Germany			
Wednesday Morning				
Time	Session 22 Simulation and Modeling of Global Interconnect	Session 23 Noise Issues in IC Design	Session 24 Analog Techniques	Session 25 General Purpose and Application Specific Digital Signal Processing
Wed. 8:30	Introduction	Introduction	Introduction	Introduction
Wed. 8:35	22.1 - The Challenge of Designing Global Signals in UDSM CMOS, (tutorial), S. Taylor, CMOS Solutions, Olga, WA	23.1 - Power Supply Noise in Future IC's: A Crystal Ball Reading (invited), P. Larsson, Bell Labs Lucent	24.1 - A Wideband Tunable CMOS Channel-Select Filter for a Low-IF Wireless Receiver, F. Behbahani et al., UCLA 24.2 - A 1V 5th-Order Bessel Filter Dedicated to Digital Standard Processes, M. Python et al., Swiss Fed. Inst. of Tech. / Rockwell	25.1 - A New Generation of DSP Architectures (invited), B. Ackland, P. D'Arcy, Lucent
Wed. 9:00				

Tues. 2:05	14.1 - Hard Disk Drive Read Channels: Technology and Trends (invited), H. Thapar et al., DataPath Systems, Los Gatos, CA	15.1 - Device and Circuit Design Issues in SOI Technology (invited), G. Shahidi et al., IBM Semi. R&D Center, Hopewell Jct., NY	16.1 - Substrate-Induced High-Frequency Noise in Deep Sub-Micron MOSFETs for RF Applications, S. Kishore et al., SiliconWave, San Diego / Rockwell, Newport Beach, CA	17.1 - IP Reuse Creation for System-on-a-Chip Design (invited), P. Bricaud, Mentor / M. Keating, Synopsys
Tues. 2:30			16.2 - RF Simulations and Physics of the Channel Noise Parameters within MOS Transistors, T. Manku et al., Univ. of Waterloo, Ontario, Canada	
Tues. 2:55	14.2 - A 450Mbit/s EPR4 PRML Read/Write Channel, M. Demicheli et al., STMicroelect. / Univ. di Pavia, Italy	15.2 - The First Copper ASICs: A 12M-Gate Technology, J. Panner et al., T. IBM, Essex Junction, VT	16.3 - Phase Noise in Oscillators: A Tutorial (invited), T. Lee, Stanford	17.2 - Owl: An Interface Description Language for IP Reuse, K. Suzuki et al., Hitachi
Tues. 3:20	14.3 - A CMOS Two-Path Tree Search Detector, X. Wang et al., UC Davis, CA	15.3 - Wireless Communication Integrated Circuits with CMOS-compatible SiGe HBT Technology Modules, (tutorial), W. Winkler et al., Inst. for Semi. Physics, Frankfurt, Germany	16.4 - Noise Analysis of a VCO with Automatic Amplitude Control, M. Margarit et al., Rockwell / Simon Fraser Univ., Vancouver / UC Berkeley	17.3 - A New Method for Reuse-Driven Design of Digital Circuits, O. Heuser et al., Fraunhofer-Inst., Duisburg, Germany
Tues. 3:45	14.4 - A 110Mhz 350mW 0.6u CMOS 16-State Generalized-Target Viterbi Detector for Disk Drive Read Channels, S. Sridharan, L. Carley, CMU			17.4 - An Integrated Environment for Configurable Designs, D. Dignam et al., GigaPixel Corp., Santa Clara, CA

Wed. 9:25	22.2 - Clock Verification in the Presence of IR-Drop in the Power Distribution Network, S. Hussain et al., Simplex Solutions, Sunnyvale, CA	23.2 - Switching Well Noise Analysis and Minimization Strategy for Low Vth CMOS Integrated Circuits, A. Koyama et al., Hitachi	24.3 - A 2Vpp Linear Input-Range Fully Balanced CMOS Transconductor and Its Application to a 2.5V 2.5MHz Gm-C LPF, T. Itakura et al., Toshiba	25.2 - A Single-Chip 1.6Billion 16-b MAC/s Multiprocessor DSP, B. Ackland et al., Lucent / MIT
Wed. 9:50	22.3 - Characterization and Modeling of Clock Skew with Process Variations, P. Zarkesh-Ha et al., Georgia Tech	23.3 - Substrate Cross Talk Noise characterization and Prevention in 0.35um CMOS Technology, J. Lee et al., National, Santa Clara, CA	24.4 - A 2.125 Gbaud 1.6kOhm Transimpedance preamplifier in 0.5um CMOS, S. Mohan, T. Lee, Stanford	25.3 - A DSP Reed-Solomon Coder, T. Wolf, TI
Wed. 10:15	22.4 - Including Inductive Effects in Interconnect Timing Analysis, B. Krauter et al., IBM, Austin, TX	23.4 - Substrate Injection and Crosstalk in CMOS Circuits, J. Briaire et al., Bell Labs Lucent / Eindhoven Univ., The Netherlands	24.5 - A 5GHz, 1mW CMOS Voltage Controlled Differential Injection Locked Frequency Divider, H. Rategh et al., Stanford	25.4 - Versatile Beamforming ASIC Architecture for Broadband Fixed Wireless Access, J.-N. Duan et al., UCLA
Wed. 10:40	22.5 - Return-Limited Inductances: A Practical Approach to On-Chip Inductance Extraction, K. Shepard et al., Columbia, NY	23.5 - A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits, R. Garpurey, TI	24.6 - A 3.25 GB/s Injection Locked CMOS Clock Recovery Cell, T. Gabara, Bell Labs Lucent	25.5 - A Single-Chip Narrowband Frequency Domain Excisor for a Global Positioning System (GPS) Receiver, P. Capozza et al., MITRE Corp., Bedford, MA
Wed. 11:05	22.6 - An Efficient Inductance Modeling for On-chip Interconnects, L. He et al., Hewlett-Packard / UCLA	23.6 - A Review of Substrate Coupling Issues and Modeling Strategies (invited), R. Singh, Cadence	24.7 - A Novel High Precision Adjustment Method for the Transconductance of a MOSFET, M. Tiilikainen, Nokia	25.6 - 470MHz Digital Filter on Delta-Sigma Modulated Signals, S. Li, D. Lewis, Univ. of Toronto

Wed. 11:30	22.7 - Mesh-Structured On-Chip Power/Ground: Design for Minimum Inductance and Characterization for Fast R, L Extraction. A. Sinha, UCLA / S. Chowdhury, Motorola, Austin, TX			
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Wed. 4:05	26.7 - Substrate Network Modeling for CMOS RF Circuit Simulation. S. Tin, K. Mayaram, Wash. St. Univ.	27.7 - A 1.5 GHz, Sub-2mW CMOS Dual-Modulus Prescaler. A. Benachour et al., Texas A&M / Rockwell		29.7 - A 1V 900MHz Image-Reject Downconverter in 0.5um CMOS. J. Long et al., Univ. of Toronto / Nortel, Ottawa
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Wednesday Afternoon				
Time	Session 26 Device and Substrate Analysis and Circuit Synthesis	Session 27 Custom Circuit Techniques for Communication Applications	Session 28 SOC Core Integration and On-Chip Communication	Session 29 RF Building Blocks for Wireless Communications
Wed. 1:30	Introduction	Introduction	Introduction	Introduction
Wed. 1:35	26.1 - Wave Pipelining YADDs - A Feasibility Study, A. Mukherjee et al., UC Santa Barbara	27.1 - Low-Power Bit-Serial Viterbi Decoder for 3rd Generation W-CDMA Systems, H. Suzuki et al., Kawasaki Steel Corp. / Univ. of Minnesota	28.1 - VSIA Technical Challenges (invited), H. Sachs et al., Fujitsu / VSIA	29.1 - Design of High-Q Varactors for Low-Power Wireless Applications using a Standard CMOS Process, M. Porret et al., Swiss Fed. Inst. of Tech. / Rockwell
Wed. 2:00	26.2 - Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSIs, K. Kanda et al., Univ. of Tokyo	27.2 - A Low-Power Direct Digital Frequency Synthesizer Architecture for Wireless Communications, A. Bellaouar et al., Univ. of Waterloo, Ontario, Canada		29.2 - A 1.3GHz CMOS VCO with 28% Frequency Tuning, F. Svelto et al., Univ. di Bergamo / Univ. di Pavia, Italy

Wed. 2:25	26.3 - ANACONDA: Robust Synthesis of Analog Circuits via Stochastic Pattern Search, R. Phelps et al., CMU / TI	27.3 - A Low-Power and Low-Noise CMOS Prescaler for 900 MHz to 1.9 GHz Wireless Applications, W-H. Chang et al., Rockwell, Thousand Oaks, CA	28.2 - An Efficient Bus Architecture for System-on-Chip Design, B. Cordan, Palmchip Corp., Loveland, CO	29.3 - A Quarter-Micron CMOS, 1GHz VCO/Prescaler-Set for Very Low Power Applications, D. Pfaff et al., Swiss Fed. Inst. of Tech.
Wed. 2:50	26.4 - Circuit Partitioning by Quadratic Boolean Programming for Reconfigurable Circuit Boards, Y. Choi, C. Rim, Sogang Univ., Seoul, Korea	27.4 - Giga Bit Per Second Per Pin Differential CMOS Circuits for Pseudo ECL Signaling, H. Djahanshahi et al., Univ. of Toronto / Vitesse Semi.	28.3 - A Bus Architecture Centric Configurable Processor System, S. Winegarden, Triscend Corp., Mountain View, CA	29.4 - Fully Integrated Low Phase-Noise PLLs Using Closed-Loop Voltage-to-Frequency Converter Architectures, A. Hafez et al., Univ. of Waterloo, Ontario, Canada
Wed. 3:15	26.5 - Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment, M. Nagata et al., Hiroshima Univ.	27.5 - A Cyclic CMOS Time-to-Digital Converter with Deep Sub-Nanosecond Resolution, P. Chen, S-I. Liu, Nat. Taiwan Univ., Taipei	28.4 - Minimizing the Effect of the Host Bus on the Performance of a Computational RAM Logic-in-Memory Parallel-Processing System, P. Nyasulu et al., Carleton Univ., Ottawa / Univ. of Alberta, Edmonton	29.5 - A Wideband Quadrature LO Generator in Digital CMOS, J. Harrison et al., Macquarie Univ., Sydney, Australia
Wed. 3:40	26.6 - An Extended Bipolar Transistor Model for Substrate Crosstalk Analysis, M. Klemme, E. Barke, Univ. of Hanover, Germany	27.6 - Frequency Scalable Non-Linear Waveform Generator for Mixed-Signal Power-Factor-Correction IC Controller, R. Zane et al., Univ. of Colorado	28.5 - The uPP ASIC: Design, Methodologies and Tools for a Pay Phone System-on-a-Chip Based on an ARM Core and Design Reuse, J. Riesco et al., Telefonica Invest. y Des., Madrid, Spain	29.6 - A 900-MHz, 0.8-um CMOS Low Noise Amplifier with 1.2-dB Noise Figure, B. Floyd et al., Univ. of FL, Gainesville