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Welcome from the CICC Committee

Welcome to CICC 2007, the 29th annual IEEE Custom Integrated Circuits Conference and leading international conference for integrated circuit development. The conference begins with a keynote address entitled "The Wireless Revolution Continues: Can Technology Keep Up with the Challenge?" by Bill Krenik, Chief Technical Officer for Texas Instruments' Wireless Terminals Business Unit. Our conference luncheon guest speaker, Paul Brokaw, from Analog Devices, provides a look at our past with his talk entitled "Growing Up With Wires & Batteries." CICC offers attendees a total educational experience with technical lecture and poster presentations, exhibits, panels, tutorials, and stimulating networking events. We cordially invite you to participate in CICC 2007 at the DoubleTree Hotel in San Jose, California.

The conference begins on Sunday, September 16 with three educational sessions taught by practicing experts working at the leading edge of their fields. The session themes are; Mixed-Signal SOC Design Methodologies, High-Speed Serial I/O Design Techniques, and Low Power Embedded ADC Design.

Monday morning Bill Krenik of Texas Instruments will address the critical technology, process and packaging challenges and solutions required to meet mobile market requirements for today and tomorrow. His presentation will provide a stimulating opening for the CICC technical program.

A record number of paper submissions in 2007 allow us to bring you a conference of the highest technical caliber. This year 198 papers were selected from 411 submitted and organized into 25 sessions. The topics addressed by these high quality papers include; analog and custom low-power circuits, wired and wireless communications, digital circuits and SoC/SiP-IP methodologies, simulation and modeling, signal and data processing, embedded memories and programmable devices, manufacturing and test, along with sensors and other emerging technologies. Highlights include invited and tutorial papers from leading experts in industry and academia.

Our Monday evening Welcome Reception and Tuesday Conference Reception are professional networking at its very best! Our exhibits area will include booths and software demonstrations from prominent industry suppliers and a lively Poster Session. The poster session is a unique forum for in-depth discussions with authors.

Monday afternoon's spirited panel discussion features experts who are sure to offer strong opinions on the topic areas: "Are Analog Designers Hopeless at Scaling? Will Digital Designers Eat Their Lunch at 45 nm and Below?"

At the conference luncheon, Paul Brokaw of Analog Devices Inc. will share with us some of the fascinating technology and characters he has encountered along the way in his talk "Growing Up With Wires & Batteries".

CICC is co-located with the IEEE Behavior, Modeling, and Simulation Conference 2007. BMAS will take place September 20 – 21 at the DoubleTree Hotel, San Jose, California. Visit the BMAS website at www.bmas-conf.org for complete conference information.

We extend our thanks to all the authors who spent many hours preparing their papers and presentations. We also wish to thank the CICC Technical Program Committee and our dedicated conference staff for all of their hard work and support. Their diligent efforts keep CICC as the best place to discover the latest in integrated circuit innovations, to hear the newest product announcements, and to debate the most effective business strategies. See you in San Jose.



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Educational Sessions

Chairperson: Laurence Nagel, Omega Enterprises

Educational Session 1 – *Mixed-Signal SOC Design Methodology*

Oak Ballroom, Sunday, September 16

Organizer: Laurence Nagel, Omega Enterprises
Co-Organizer: Henry Chang, Designer's Guide Consulting

8:00 – 9:50

E1-1 Top-down Design Methodology

Scott Shelton, Cadence Analog Design Services

Mixed-signal design at the SOC level necessitates a top-down mixed signal design methodology to meet today's project schedules with successful end products. This technical discussion examines methods for successfully handling the analog and digital domain interactions in large complex ICs with today's tools; crafting and executing a simulation strategy which efficiently verifies functionality and performance; and efficiently modeling at appropriate levels of abstraction. The discussion is presented within the context of actual designs by some of Cadence's internal design teams, and examines how they have shaped and melded the methodologies as presented. Given the diverse skill sets and multiple IP vendors garnered for SOCs, the structure and management of these design teams throughout the various project stages is explored as well. The session covers these topics through the complete design cycle, from project kickoff to IP block delivery for integration or SOC tapeout.

10:10 – 12:00

E1-2 High-Performance Energy-Efficient Digital Design Technologies for Nanoscale SOC

Ram Krishnamurthy, Intel

This presentation examines some of the prominent barriers to high-performance and energy-efficient digital design in the sub-65nm CMOS regime and outlines new paradigm shifts necessary for next-generation SOC digital design and methodologies. Emerging trends in SOC industry including special-purpose multimedia/communication accelerators, networks-on-chip, co-processor arrays, and reconfigurable DSP and their associated power-performance trade-offs are reviewed. Energy-efficient data-path and interconnect circuit techniques, variation-tolerant design methods, static/dynamic supply scaling, ultra-low-voltage circuits, and multi-supply/multi-threshold design and supply gating methodologies for switching and leakage energy reduction are described. Special purpose hardware accelerators and SOC building blocks for enabling high performance-per-Watt on specialized DSP tasks such as encryption and media processing are presented. Many chip design examples and their results will be discussed as part of this presentation.

1:00 – 2:50

E1-3 Top-down Design of RF Transceivers using VHDL

Khurram Waheed, Texas Instruments

RF transceivers comprise a particularly difficult challenge in SOC design because their proper operation requires correct interoperability of RF subsystems, analog subsystems, and digital subsystems. This presentation describes the numerous challenges in the top-down design of a RF transceiver SOC and describes how VHDL simulation is in the design flow. Case studies of RF transceiver chips designed at Texas Instruments are used to illustrate how the design challenges were overcome to produce working SOCs.

3:10 – 5:00

E1-4 Analog Verification

Ken Kundert, Designer's Guide Consulting

Verification is becoming recognized as one of the most important issues when designing large analog circuits, and as a result design methodologies are starting to change. This change mirrors a change that occurred in digital design 10-15 years ago. In this presentation I will show why the problem has become so significant, and what people are doing to control the problem.

Educational Session 2
High-Speed Serial I/O Design Techniques
Fir Ballroom, Sunday, September 16

Organizer: Ramesh Harjani, University of Minnesota
Co-Organizer: Gordon Roberts, McGill University

8:00 – 9:30

E2-1 Introduction to High-speed I/O
Randy Mooney, Intel

I'll discuss the constraints of the design space for microprocessor platforms, then take a look at the state of the technologies required to deliver bandwidth in these platforms. These technologies include analysis tools, interconnect components, modulation and equalization choices that fit the constraints, and the various circuits required in silicon. I'll then take a look at future platform requirements, and the potential solution space to meet those needs.

9:30 – 11:00

E2-2 Introduction to Signal Integrity
Bob Sainati, 3M

The demand for ever increasing data rates in today's electronic systems requires the use of shorter rise time signals and faster clock speeds. Both data and clock signals are conveyed using interconnects to carry signals on-chip, on a multilayer pc board, through backplanes or via cables. This tutorial focuses on the impact of interconnects on high speed digital signals. Here the term interconnect refers not only signal traces but packaging, connectors, vias, etc. Shorter rise times, of course, imply wider frequency bandwidths. Many traditional interconnect design techniques focus on factors such as routing efficiency, mechanical and thermal issues. Because of this, many interconnect schemes lack the bandwidth necessary to distribute high speed signals faithfully. Likewise faster rise times increase the probability of significant crosstalk between multiple nets. Similar issues exist with power distribution networks. Short rise time signals can require the supplying of large amounts of current within a very short time. Improper design of power distribution networks can create distortion producing supply voltage drops. Finally, the higher frequencies of short rise time signals are much more easily radiated thus resulting in potential EMI/EMC problems.

Techniques such as the use of microwave measurement techniques (e.g., network analyzers), transmission line theory, microwave scattering parameter analysis and electromagnetic simulators have been adopted in order to design improved interconnects and power distribution networks. These techniques all have at least some basis in electromagnetic theory, that is, Maxwell's equations. Although it is common to think of digital signals in terms of voltages and currents, ultimately they are a set of (coupled) electric and magnetic fields surrounding the metallization of signal traces, connector and package pins, via metallization, etc. Many of the issues associated with signal integrity are a result of the finite velocity of the fields when guided by traces, the propensity of fields to locally store energy in regions where abrupt changes in geometry, direction, etc. are encountered and the fact that crosstalk and radiation increase because a fixed physical size becomes electrically larger as the wavelength decreases. The intent of this course is to link the physics of electromagnetic fields to the signal behavior observed on

an interconnect. For instance, quantities such as inductance and capacitance are fundamentally described in terms of fields. Also guided electromagnetic waves are the foundation of transmission line theory and scattering parameters. This course will not be a detailed exposition of electromagnetic theory but rather a review of concepts and an application of them to high speed digital signal interconnect behavior.

11:00 – 12:00 and 1:00 – 2:00

E2-3 Jitter Analysis

Mike Li, Wavecrest

In this tutorial presentation, we will first review where the technology is heading to for the multiple Gbps high-speed links and I/O buses for devices and systems in networks and computers. Second, we will discuss why jitter and signal integrity have become the major challenges, as well as limiting factors for developing those high-speed, high performance, and more increasingly, high volume link devices and systems. Third, we will discuss the jitter and signal integrity modeling, simulation, verification and characterization methodologies for jitter and signal integrity within the context of a serial link. We will cover these ever evolving cutting edge topics from generic perspective, as well as practical application perspective, with real-world examples from multiple Gbps link technologies of PCI Express, FB DIMM, and Serial ATA in computer I/Os, and Fibre Channel and Gigabit Ethernet in networks.

2:00 – 3:30

E2-4 Circuit/System Aspects of I/O Equalization

Vladimir Stojanovic, Massachusetts Institute of Technology

Today's high-speed interfaces are limited by the bandwidth of the communication channel, tight power constraints and noise sources that differ from those in standard communication systems. The wire bandwidth limitations make straight circuit solutions inefficient, and the power and area constraints make standard digital communication approaches infeasible. Efficient solutions require bridging the fields of digital communications, optimization, statistical and dynamic system modeling, with system architecture, mixed-signal and digital circuit design.

This tutorial covers the circuit and system design of equalized high-speed I/Os. We start by introducing the basics of channel properties, modeling, measurements, and communications techniques. We then focus on different link equalization techniques, comparing them both from system perspective and from the performance of resulting circuit implementations. Some examples will cover trade-offs between transmit pre-emphasis and decision-feedback equalization, linear analog receiver equalization as well as joint modulation/equalization and equalization/coding techniques (like PAM4, duobinary and multitone signaling). Implementations of transmitter FIR equalizers, several DFE receiver topologies and peaking amplifiers will be discussed in detail. Several adaptive techniques for equalizer tuning and link monitoring will also be presented.

3:30 – 5:00

E2-5 Clocking and CDRs

Jafar Savoj, Rambus

High-purity clock generation enables longer reach in wired communication systems. Optical and copper standards set an upper bound on the noise and distortion that can be added to the signal at the source. This tutorial describes means of efficient clock generation and distribution in high-performance chips to satisfy requirements imposed by the standards. Clock and data recovery (CDR) circuits are an integral part of wired communication systems. With the accelerated rate of device scaling in recent decades, CDR architectures have transitioned from fully analog into mixed-mode and digital implementations. The tutorial later addresses the evolution of CDR architectures, as well as the design of its building blocks.

Educational Session 3

Low Power Embedded ADC Design

Pine Ballroom, Sunday, September 16

Organizer: Sang-Soo Lee, Pixelplus

Co-Organizer: Shahriar Mirabbasi, University of British Columbia

8:00 – 9:50

E3-1 System Aspects

Thomas Cho, Marvell

Aggressive CMOS scaling in the last couple of decades has enabled powerful DSP engines for many digital communication systems in both wireless and wired-line applications. But the world is still analog, and the requirements for the analog-to-digital interface circuits are becoming increasingly stringent not to limit the overall system performance. In addition, A/D converters, which used to be discrete components on the board in the past, are now being integrated onto an IC together with many other functions for smaller form factors, bringing new challenges to analog circuit designers. This tutorial will give an overview of both circuit and system level requirements for the embedded A/D converters used in various wireless/wired-line applications. Practical considerations for system-on-chip environments, such as on-chip reference generation, noise isolation, low-power/low-voltage designs, testing, and other challenges will also be discussed.

10:10 – 12:00

E3-2 Pipeline ADC Design

Boris Murmann, Stanford University

Pipelined analog-to-digital converters have evolved as a popular architecture for broadband quantization in applications requiring 8-14 bit resolution and sampling rates up to several hundred MS/s. This lecture discusses the design and implementation of pipelined ADCs using a top-down approach, ranging from an architecture level analysis to transistor level implementation details. Specific topics include: (1) Basic operation principle, (2) Redundancy and digital calibration techniques, (3) Error and noise budgeting; pipeline stage scaling and choice of per-stage resolution, (4) Transistor level circuit implementation; low power techniques such as OTA sharing and SHA-less front-ends, and (5) Performance survey; recent trends and developments in research.

1:00 – 2:50

E3-3 Sigma Delta ADC

Katelijjn Vleugels, H-Stream Wireless

In this talk, we will look at the various aspects of Sigma-Delta Analog-to-Digital Converter (ADC) design. We begin with a review of the basic concepts of Sigma-Delta data converters, followed by an overview of state-of-the art Sigma-Delta ADC implementations. Several architectures exist, and the optimal architecture heavily depends on the system requirements imposed by the application. The advantages and challenges of various architectures are discussed next. We then look at the impact of circuit implementation non-idealities on the overall ADC performance. The talk will conclude with an example of a Sigma-Delta ADC design.

3:10 – 5:00

E3-4 Case Study

Stacy Ho, Analog Devices

This talk will present case studies on embedded ADC design for mobile handsets. Factors that influence the selection of ADC architecture, such as power dissipation, wireless standards requirements, and cost, will be discussed. Issues due to the system level integration of ADCs will be addressed, such as:

coexistence with digital baseband and power management blocks, architectural tradeoffs, reference and clock requirements. The talk will also review published embedded ADCs for wireless applications.

Technical Sessions

Monday, September 17 – Wednesday, September 19

Session 1 – Keynote Presentation

Oak Ballroom, Monday Morning, September 17

8:15 am **Welcome and Opening Remarks**
Awards Presentations
Keynote Speaker Introduction
Larry Wissel, General Chairman

8:30 am **Keynote Presentation**

“The Wireless Revolution Continues:
Can Technology Keep Up with the Challenge?”

Dr. Bill Krenik, Chief Technical Officer for Texas Instruments' Wireless Terminals Business Unit

The exploding market for consumer electronics is creating diverse product opportunities, with many products demanding unique technology features to enable successful performance, power-efficiency, size and cost. The wireless market is a high-growth market, and a critical driver of technology innovations. Whether creating a cutting-edge mobile phone with the hottest features or a modest handset required for high-growth emerging economies, a mobile designer is increasingly more challenged to satisfy product goals with existing technology. From the perspective of the industry-leading semiconductor provider entrenched in the wireless space, Bill Krenik, Chief Technical Officer for TI's Wireless Terminals Business Unit, will address the critical technology, process and packaging challenges and solutions required to meet mobile market requirements for today and tomorrow.



Session 2 –3D and SiP

Oak Ballroom, Monday Morning, September 17

Chair: Rakesh Patel
Co-Chair : Ann Rincon

Two invited papers on 3D wireless high performance interchip communications using capacitive and inductive interconnect techniques are presented. In addition, resonant clocking in CMOS is explored for active jitter deskewing.

10:00 am
Introduction

2.1

10:05 am
3D Capacitive Interconnections for High Speed Interchip Communication (INVITED PAPER), R. Canegallo, L. Ciccarelli, P.L. Rolandi, STMicroelectronics, A. Fazzi, L. Magagni, F. Natali, R. Guerrieri University of Bologna, E. Jung, IZM Fraunhofer, L. Di Cioccio, CEA-LETI

A 3D Interconnection scheme based on capacitive coupling for high speed chip to chip communication has been implemented in a 0.13 μm CMOS process. This work shows, with a synchronous approach data transmission at 900MHz with electrodes $15 \times 15 \mu\text{m}^2$ and energy consumption of 41fJ/bit. With asynchronous approach we demonstrate with electrodes $8 \times 8 \mu\text{m}^2$ a propagation of clock at 1.7GHz and a propagation delay of 420ps for general purpose signal with energy consumption of 80fJ/bit.

2.2

10:55 am

Low-Jitter Active Deskewing Through Injection-Locked Resonant Clocking, Z. Xu and K. Shepard, Columbia University

Active deskewing is an important technique for managing variability in clock distributions but introduces latency and power-supply-noise sensitivity to the resulting networks. In this paper, we demonstrate how active deskewing can be achieved with resonant distributions without introducing significant jitter. The prototype network operates at a nominal 2-GHz frequency in a 0.18 μm CMOS technology with more than 25 pF/ mm^2 of clock loading.

2.3

11:20 am

Wideband Inductive-coupling Interface for High-performance Portable System (INVITED PAPER), H. Ishikuro, N. Miura and T. Kuroda, Keio University

This paper presents a wideband, low power, and low cost pulse-based inductive-coupling interface for wireless data transfer in high performance portable devices. General aspects of wireless links are discussed to understand the position of inductive-coupling technique. Two applications of the inductive-coupling links are introduced. One is a 0.14pJ/b inter-chip link for System-in-a-Package. The other is a detachable wireless interface for chip monitoring through LSI package. Circuit design techniques for power reduction and an extension of communication range are presented.

Session 3 – Extreme SRAMs

Fir Ballroom, Monday Morning, September 17

Chair: Takashi Akioka

Co-Chair: Tom Andre

These papers explore state-of-the-art SRAMs as well as new structures and analysis techniques to enable SRAM scaling into future technology generations.

10:00 am

Introduction

3.1

10:05 am

A 550ps Access-Time Compilable SRAM in 65nm CMOS Technology, L. Wissel, H. Pilo, C. LeBlanc, X. Wang, S. Lamphier and M. Fragano, IBM

A fixed-configuration custom SRAM macro with a highly-scalable architecture was used as the basis for an ASIC SRAM compiler. The 256Kb fixed-configuration uses dynamic circuitry [1] and other design techniques, and has been demonstrated in silicon to have an access time of 550ps. The compilable SRAM extends the column mux options, and can be compiled from 2Kb to 1.1Mb. Novel circuitry is used for efficient redundancy implementation in both the row and column dimensions.

3.2

10:30 am

A Disturb Decoupled Column Select 8T SRAM Cell, V. Ramadurai, R. Joshi and R. Kanj, IBM

This paper presents a novel 8T SRAM cell that provides a way to eliminate the column select read disturb scenario. The 8T cell is then used in conjunction with a sense-amp based architecture that minimizes read disturb to selected cells. Fabricated hardware results and simulation of this architecture show improvements of cell V_{ddmin} over traditional 6T cells by more than 150mV for 90nm PD/SOI technology.

3.3

10:55 am

Canary Replica Feedback for Near-DRV Standby V_{DD} Scaling in a 90nm SRAM, J. Wang and B. Calhoun, University of Virginia

Canary bitcells act as monitors in a feedback architecture to sense the proximity to the Data Retention Voltage (DRV) for SRAM bitcells during standby voltage scaling. This approach implements aggressive standby VDD scaling by tracking PVT variations and gives the flexibility to tradeoff between reliability and leakage power savings. A 90nm SRAM test chip confirms the function of this closed-loop approach. Power savings improve by up to 30x compared with the conventional guard-banding approach.

3.4

11:20 am

Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology, S. O'uchi, M. Masahara, K. Sakamoto, K. Endo, Y.X. Liu, T. Matsukawa, T. Sekigawa, H. Koike and E. Suzuki, National Institute of AIST

We propose a flex-pass-gate SRAM (Flex-PG SRAM), i.e., a FinFET-based SRAM to enhance both the read and write static noise margins (SNMs) independently. The flip-flop in the Flex-PG SRAM consists of usual FinFETs while its pass gates consist of double-“independent”-gate FinFETs, four-terminal-FinFETs. A TCAD simulation revealed that the Flex-PG SRAM increases the read SNM by 70 mV even when its 6-sigma tolerance is ensured, without the cell size penalty and decrease in the write SNM.

3.5

11:45 am

Simple Statistical Analysis Techniques to Determine Minimum Sense Amp Set Times, R. Houle, IBM

Simple statistical analysis techniques are described, involving a relatively small number of actual circuit simulations, to accurately determine the minimum required sense amp set time for memory designs. Techniques to generate and evaluate the statistical distributions for signal development, leakage and sense amp asymmetry are discussed with important implications to sense amp design.

Session 4 – Compact Models for Advanced CMOS Technologies

Pine Ballroom, Monday Morning, September 17

Chair: Brian Chen

Co-Chair : Hidetoshi Onodera

Two invited papers present next-generation compact models of advanced SOI and multiple gate MOSFETs, followed by a regular paper on characterization and modeling of 65nm copper interconnect resistance.

10:00 am

Introduction

4.1

10:05 am

PSP-SOI: A Surface Potential Based Compact Model of Partially Depleted SOI MOSFETs (INVITED PAPER), W. Wu, X. Li, G. Gildenblat, Arizona State University, G. Workman, S. Veeraraghavan, C. McAndrew, Freescale Semiconductor, R. van Langevelde, Philips, G. Smit, D. Klaassen, A. Scholten NXP Semiconductors and J. Watts, IBM

This paper reports recent progress on partially depleted (PD) SOI modeling using a surface potential based approach. The new model, called PSP-SOI, is formulated within the framework of the latest industry standard bulk MOSFET model PSP. In addition to its physics-based formulation and scalability inherited from PSP, PSP-SOI captures SOI specific effects by including a floating body simulation capability, a parasitic bipolar model, and self-heating. A nonlinear body resistance is included for modeling body-contacted SOI devices. The PSP-SOI model has been extensively tested on several PD/SOI technologies.

4.2

10:55 am

Charge-Based Compact Modeling of Multiple-Gate MOSFET (INVITED PAPER), B. Iniguez, A. Lazaro, H. Abd El Hamid, O. Moldovan, B. Nae, URV, J. Roig, LAAS and D. Jimenez, UAB

We present new compact modeling techniques which have been applied for different types of multiple-gate MOSFETs. Long channel models are obtained by deriving a unified charge control model from the solution the 1-D Poisson's equation. Scalable models for the short-channel effects have been developed by solving the 2-D or 3-D Poisson's equation. We observed a very good agreement with numerical simulations of the characteristics of different multiple-gate devices. We also extended our compact models to the high frequency operation.

4.3

11:45 am

Characterization, Modeling and Extraction of Cu Wire Resistance for 65 nm Technology, N. Lu, M. Angyal, G. Matusiewicz, V. McGahay and T. Standaert, IBM

We present an innovative and comprehensive approach to characterize and model interconnect resistance. We measured and analyzed Cu wire resistance data for multiple wire widths on 10 BEOL levels at multiple temperatures and, with SEM cross-section data, extracted all model parameters in IBM 65nm technology. The extracted SPICE wire resistance model includes the congregated effects of surface scattering, grain boundary scattering and surface roughness. New behavior of wire resistance is reported for the first time.

Session 5 – Oversampling A/D Converters

Cedar Ballroom, Monday Morning, September 17

Chair: Jennifer Lloyd

Co-Chair: Un-Ku Moon

This session highlights recent advances in oversampling ADCs including dynamic range improvements for both bandpass and lowpass modulators and improved tolerance for analog imperfections.

10:00 am

Introduction

5.1

10:05 am

A 63-mA 112/94-dB DR IF Bandpass Delta-Sigma Modulator with Direct Feed-forward and Double Sampling, T. Yamamoto, M. Kasahara and T. Matsuura, Renesas Technology Corp.

We developed a 10.7-MHz IF bandpass discrete-time 4th-order 4-bit delta-sigma modulator for AM/FM car radio tuners. Using direct feed-forward and double sampling, we have achieved a dynamic range (DR) of 112 dB in the 3-kHz AM bandwidth (BW) and a DR of 94 dB in the 200-kHz FM BW. The modulator occupies 3 mm², in 0.15 μm CMOS technology, and draws 63 mA of current.

5.2

10:30 am

A Delta-Sigma Modulator with a Widely Programmable Center Frequency and 82-dB Peak SNDR, K. Yamamoto, A. Chan Carusone and F. Dawson, University of Toronto

A 4-bit fourth-order delta-sigma modulator with a widely programmable center frequency is presented. Novel methods for quantizing and implementing the digitally programmable modulator coefficients enable performance comparable to state-of-the-art discrete-time fixed-frequency modulators at any center frequency from dc to 0.31fs in steps of 0.0052fs. The 0.18-μm 1.8-V CMOS prototype consumes 115 mW at a sampling frequency of 40 MHz. The peak SNDR and SNR over a 310-kHz bandwidth are 82 dB and 86 dB respectively.

5.3

10:55 am

A 94dB SFDR 78dB DR 2.2MHz BW Multi-bit Delta-Sigma Modulator with Noise Shaping DAC, J. Chen and Y.P. Xu, National University of Singapore

A 5th-order multi-bit lowpass delta-sigma modulator employs a proposed noise shaping dynamic element matching (NSDEM) technique to remove DAC non-linearity error. Unlike most existing DEMs trading SNR for SFDR, the proposed technique improves both SFDR and SNR. The noise shaping is incorporated in the first integrator of the loop filter without any additional analog circuitry. The fabricated modulator chip achieves 94dB SFDR and 78dB DR in 2.2MHz BW and meets the ADSL2+ specifications.

5.4

11:20 am

A 18mW CT Sigma-Delta Modulator with 25MHz Bandwidth for Next Generation Wireless Applications, X. Chen, Y. Wang, G. Temes, Oregon State University, Y. Fujimoto, P. Lo Ré, Y. Kanazawa, Sharp Corp., J. Steensgaard, Esion LLC

The design of a wideband low-power continuous-time (CT) Delta-Sigma modulator is presented in this paper. A modified feed-forward architecture is proposed to realize the low-power loop filter as well as cancel the out-of-band peaking in the signal transfer function. Several high-speed low-power design techniques are used in the circuits. The modulator achieves 60 dB dynamic range (DR) within 20 MHz signal bandwidth, and 55 dB DR within 25 MHz signal bandwidth. Clocked at 400 MHz, the modulator consumes only 10 mA current from a 1.8 V supply.

5.5

11:45 am

Multi-Bit Sigma Delta ADC with Reduced Feedback Levels, Extended Dynamic Range and Increased Tolerance for Analog Imperfections, J.-Y. Wu, R. Subramoniam, Z. Zhang, A. Djabbari, P. Holloway, M. Yousefi, M. Aslan, H. Hong and A. Bahai, National Semiconductor, F. Maloberti, University of Pavia

A novel second order sigma delta modulator (SDM) with 5-bit quantizer has been proposed with simplified DAC arrays, high-order truncation noise shaping for increased tolerance to analog imperfections, and extended dynamic range for a maximum input signal swing of up to -0.45dBFS. With truncation filter and pseudo SDM in the DSP, the truncation and saturation errors are compensated through the DAC arrays and the DSP. The design was fabricated in 0.18μ Dual Gate Oxide (DGO)

process. A SNDR (Signal-to-Noise-and-Distortion Ratio) of 98.4 dB and a SNR (Signal-to-Noise Ratio) of 108-dB were measured for a 31.25-KHz signal bandwidth at 8-MHz sampling frequency with a power consumption of about 14.7 mW.

Session 6 – Advances in Programmable Devices

Oak Ballroom, Monday Afternoon, September 17

Chair: Raj Amirtharajah

Co-Chair: Steve Wilton

Programmable devices are everywhere: from consumer products to high-security applications. This session highlights novel architectures, new CAD techniques, and innovative technologies that make these systems possible.

1:30 pm

Introduction

6.1

1:35 pm

Coarse-Grained Reconfigurable Image Stream Processor for Digital Still Cameras and Camcorders, J. C. Chen, S.-Y. Chien, National Taiwan University, C.-F. Shen, VIVOTEK

A 345Mpixels/s coarse-grained reconfigurable image stream processor (CRISP) is proposed and implemented with 5mm² area in 0.18μm CMOS technology for the image pipelines of digital still cameras and video camcoders. The novel CRISP architecture with scalable reconfigurable stage processing elements and reconfigurable interconnection could achieve high processing speed at low cost, while satisfying the flexibility and performance requirements of high-end image preprocessing for 10M-pixel scale still cameras and 1920x1080 camcoders.

6.2

2:00 pm

CAD Techniques for Power Optimization in Virtex-5 FPGAs, S. Gupta, J. Anderson, L. Farragher and Q. Wang, Xilinx, Inc.

We consider dynamic power dissipation in FPGAs and present CAD techniques for dynamic power reduction. The proposed techniques, comprising power-aware placement, routing, and a novel post-routing transformation, are applied to optimize the power consumed by industrial designs implemented in the Xilinx Virtex-5 FPGA. Board-level power measurements on a suite of industrial designs show that the techniques reduce power by 10%, on average.

6.3

2:25 pm

Flash-based Field Programmable Gate Array Technology with Deep Trench Isolation, K.J. Han, N. Chan, S. Kim, B. Leung, V. Hecht, B. Cronquist, Actel, D. Shum, A. Tilke, L. Pescini, M. Stiftinger and R. Kakoschke, Infineon

A highly scalable flash-based Field Programmable Gate Array (FPGA) technology has been achieved with Deep Trench Isolation (DTI). The DTI allows for a reduced cell size and enables Independent Pwell (IPW) operation. The IPW allows the Fowler-Nordheim (FN) Uniform Channel Program and Erase (UCPE) with less than ±10V. Additionally, the IPW approach allows a greater flexibility in the array bias scheme reducing the gate disturb during programming and eliminating all Gate-Induced Drain Leakage (GIDL) conditions. Characterization of a FPGA cell and 0.5 Mbit array with 90nm design rules is demonstrated with excellent electrical characteristics.

6.4

2:50 pm

Analysis of Data Remanence in a 90nm FPGA, T. Tuan, T. Strader and S. Trimberger, Xilinx, Inc.

FPGAs are increasingly used in military applications where security is paramount. In this paper, we study data remanence in modern FPGAs using a custom 90nm FPGA designed for this test. The effects of temperatures, architecture, memory topology, and power off methods are analyzed. We find remanence properties in FPGAs to depend on architecture and data content. To our knowledge, this is the first study of data remanence in FPGAs and in deep-submicron ICs.

3:15 pm - Break

Session 7 – Emerging Wireless Applications

Fir Ballroom, Monday Afternoon, September 17

Chair : Stefan Drude

Co-Chair : Earl McCune

Progress in achieving high levels of integration is presented for single chip solutions in satellite TV, WiMax-WiBRO, GPS, and RFID applications, using a variety of process technologies.

1:30 pm

Introduction

7.1

1:35 pm

A Single-Conversion SiGe BiCMOS Satellite TV LNB Front-End Using an Image Reject Mixer and a Calibrated Full-Rate VCO, A. Maxim, M. Gheorghe, D. Smith, Maxim, Inc.

A fully-integrated satellite TV down-converter was realized in a 0.18 μm SiGe BiCMOS process that provides both 70GHz ft NPN HBTs used for the main signal path and 0.18 μm CMOS FETs used for the frequency synthesizer reference clock path and LC-VCO frequency calibration circuitry. A low phase-noise, low tuning gain 10GHz LC-VCO that covers both low and high Ku-bands was realized by combining a 30% discrete steps frequency calibration with a 2% continuous frequency tuning. Offset-biased accumulation MOS varactors provide a virtually constant tuning gain by summing shifted C(V) curves that are uniformly distributed over the entire control voltage range. The on-chip synthesizer loop filter eliminates the sensitivity to off-chip noise and spur coupling. Mixer's noise was reduced by using an image-reject architecture that attenuates the thermal noise contribution from the image frequency. The LNB performance includes: <6dB noise figure, 18dBm output IP3, -106dBc/Hz phase noise at 100KHz offset, <0.4 rms total integrated phase noise, 1.7x1.5mm² die area and 125mA bias current from a 3.3V supply.

7.2

2:00 pm

A Low Power, High Performance BiCMOS MIMO/Diversity Direct Conversion Transceiver IC For WiBro/WiMAX (802.16e) (INVITED PAPER), M. Locher, M. Tomesen, J. Kuenen, A. Daanen, H. Visser, B. Essink, P.P. Vervoort, M. Nijrolder, R. Kopmeiners, W. Redman-White, R. Balmford, R. El Waffaoui, NXP Semiconductors

This paper describes a MIMO, low power, high performance direct conversion WiBro/WiMAX 802.16e radio transceiver optimized for mobile applications and coexistence with on-board Cellular and ISM-band systems. It is fabricated in a SiGe BiCMOS process and achieves a receiver NF of less than 2.5dB over an operation frequency of 2.3-2.7GHz. The transmit gain can be digitally tuned over a 75dB range. The transceiver consumes 65/103mA at a 2.8V supply in OFDMA Rx/Tx modes respectively.

7.3

2:25 pm

A Low-IF CMOS Simultaneous GPS Receiver Integrated in a Multimode Transceiver, Y. Xu, K. Wang, T. Pals, A. Hadjichristos, K. Sahota and C. Persico, Qualcomm, Inc.

This paper describes a low-IF GPS receiver circuit that operates simultaneously with WCDMA/CDMA2000 transceivers. The RF front-end circuit dynamically adjusts the linearity performance based on the instantaneous transmitting power of the integrated transmitter. The receiver measured performances are >80dB gain, 2.0dB noise figure, maximum out-of-band IIP3 is +6dBm. The receiver is fabricated in a 0.18 μ m RFCMOS process, and draws 36.7mA at high linearity mode and 27.4mA at low linearity mode using switch mode power supply.

7.4

2:50 pm

A Single-Chip UHF RFID Reader in 0.18 μ m CMOS, W. Wang, S. Lou, K. Chui, S. Rong, C.-F. Lok, H. Zheng, H.T. Chan, S.W. Man, H.C. Luong, V.K. Lau and C.-Y. Tsui, Hong Kong University of Science and Technology

An 860MHz-960MHz UHF RFID reader is designed in 0.18 μ m CMOS that fully integrates an RF transceiver and a digital baseband. Highly reconfigurable mixed-signal baseband architecture for channel selection filtering is proposed to achieve optimal power consumption for multi-protocol operation with different system dynamic ranges and data rates. In the talk mode with LNA bypassed, the RX measures a sensitivity of -70dBm in the presence of a -5dBm self-interferer. In the listen mode, LNA is turned on, and RX sensitivity of -90dBm is measured. The TX achieves output power from -9 to 11dBm with output P-1dB of 10.4dBm.

3:15 pm - Break

Session 8 – Microsystems for BioMedical Applications

Pine Ballroom, Monday Afternoon, September 17

Chair: Dawn Fitzgerald

Co-Chair : Sudhir Aggarwal

A tutorial on the acquisition of biopotentials is presented followed by three papers on emerging microsystems for biomedical applications. These include circuit innovations in MRI, hearing aid and tactile imaging.

1:30 pm

Introduction

8.1

1:35 pm

A Versatile Integrated Circuit for the Acquisition of Biopotentials (INVITED PAPER), R. Harrison, University of Utah

Electrically active cells in the body produce a wide variety of voltage signals that are useful for medical diagnosis and scientific investigation. These biopotentials span a wide range of amplitudes and frequencies. We have developed a versatile front-end integrated circuit that can be used to amplify many types of bioelectrical signals. The 0.6- μ m CMOS chip contains 16 fully-differential amplifiers with gains of 46 dB, 2 μ Vrms input-referred noise, and bandwidths programmable from 10Hz to 10kHz.

8.2

2:00 pm

A Spectral-Scanning Magnetic Resonance Imaging (MRI) Integrated System, A. Hassibi, University of Texas, A. Babakhani and A. Hajimiri, California Institute of Technology

An integrated spectral-scanning magnetic resonance imaging (MRI) technique is implemented in a 0.12 μm SiGe BiCMOS process. This system is designed for small-scale MRI applications with non-uniform and low magnetic fields. The system is capable of generating customized magnetic resonance (MR) excitation signals, and also recovering the MR response using a coherent direct conversion receiver. The operation frequency is tunable from DC to 37MHz for wide-band MRI and up to 250MHz for narrow-band MR spectroscopy.

8.3

2:25 pm

A Real-Time Feedback Controlled Hearing Aid Chip with Reference Ear Model, S. Kim, S.J. Lee, N. Cho, S.-J. Song and H.-J. Yoo, KAIST

A real-time hearing aid chip with the reference ear model (REM) and the comparison processor (COMP) is proposed and implemented. Through the COMP the response differences between the reference ear model and the impaired ear of the patient are achieved and processed to compensate the hearing loss of the patient. By adopting this architecture, the fully internal gain fitting and verification of the hearing aid with only single initial hearing loss test is implemented. To reduce the power dissipation and achieve the high flexibility, the preamplifier which has programmable multi threshold voltages is introduced. The feedback controlled hearing aid chip is implemented in 0.18 μm CMOS technology, consumes less than 110 μW and has a die size of 3.7 mm^2 .

8.4

2:50 pm

Multi-functional Monolithic-MEMS Tactile Imager Using Flexible Deformation of Silicon IC, H. Takao, M. Yawata, R. Kodama, K. Sawada and M. Ishida, Toyohashi University of Technology

In this paper, a novel device technology of multi-functional MEMS tactile imager using flexible deformation of silicon IC for advanced tactile sensing applications is investigated. Presently obtained performances of multi-functional tactile imager with sensing abilities of contact-force, hardness and temperature distributions are totally discussed for the first time. Finally, total integration design of multi-functional monolithic tactile imager is presented considering robustness of the sensor structure under practical use in tactile applications.

3:15 pm – Break

Session 9 – Test, Characterization, and Jitter of High-Speed Serial I/O and Clocks

Cedar Ballroom, Monday Afternoon, September 17

Chair: Jeanne Trinko Mechler

Co-Chair : Gordon Roberts

Characterization, test and jitter measurements are reaching picosecond resolution for high speed serial links and clock networks.

1:30 pm

Introduction

9.1

1:35 pm

Testing SerDes Beyond 4 Gbps – Changing Priorities (INVITED PAPER), S. Sunter and A. Roy, LogicVision

After briefly reviewing conventional jitter and jitter tolerance tests for SerDes, this paper shows that ISI is a dominant source of bit errors above 4 Gbps, and is inadequately tested. We demonstrate the correlation between ISI and transition-density dependent delay (TDDD) at 3.1 Gbps, and provide detailed 6.25 Gbps silicon results for an undersampling digital BIST that can measure jitter, TDDD, and other parameters at production speeds with picosecond resolution.

9.2

2:00 pm

Challenges and Solutions for Standards-Based Serial 10 Gb/s Backplane Ethernet (INVITED PAPER), A. Healey, LSI Corporation

The application of Ethernet as a fabric technology in modular platforms has led to interest in the development of a standard set of physical layer subsystems to support this practice. Recently, the IEEE 802.3ap-2007 standard, commonly referred to as Backplane Ethernet, was approved. This standard defines the electrical performance of the backplane interconnect, transmitters, and receivers required to support data rates up to 10 Gb/s per channel. This paper provides an overview of the key specifications for serial 10 Gb/s Backplane Ethernet and relates the requirements to backplane construction considerations and link performance trade-offs.

9.3

2:50 pm

2GS/s, 10ps Resolution CMOS Differential Time-to-Digital Converter for Real-Time Testing of Source-Synchronous Memory Device, K. Yamamoto, M. Suda and T. Okayasu, Advantest Corporation

A Differential Time-to-Digital Converter (TDC), fabricated in 0.18mm CMOS process, for source-synchronous device testing is demonstrated. It exhibits a maximum sampling rate of 2.133GS/s, a variable resolution of 10-40ps, an infinite measurement range, an INL of 8.5ps(pk-pk), and a jitter of 18.3ps(pk-pk). It is available to be applied to the jitter histogram measurement without dead-time because it detects all transition timing continuously. Furthermore, a possible application of this TDC to ADC or DAC is suggested.

3:15 pm – Break

9.4

3:35 pm

Optimizing Circuit Performance and ESD Protection for High-Speed Differential I/Os, H. Sarbishaei, O. Semenov and M. Sachdev, University of Waterloo

Impact of ESD protection devices on circuit operation is very important in gigahertz applications. In this paper, the impact of different ESD protection methodologies on CML drivers is discussed. ESD protection is provided using MOSFET and SCR devices. Study of the interaction between driver and ESD protection circuit shows that jitter is very sensitive to parasitics of ESD protection circuits. Furthermore, an analysis shows that substrate-triggering has less impact on jitter compared to gate-coupling

9.5

4:00 pm

Embedded Test Features for High-Speed Serial I/O (INVITED PAPER), J. Rearick, Advanced Micro Devices

High-speed serial I/O interfaces are becoming ubiquitous, yet remain very challenging to test effectively and efficiently (or even at all) during high volume production. The use of on-chip test and measurement circuitry to assist or replace external equipment is an emerging paradigm to address the issue. A brief

survey of these embedded test features and their optimization for HVM support, plus an overview of the activity of the IEEE P1687 working group, is presented.

9.6

4:25 pm

On-Chip Circuit for Measuring Period Jitter and Skew of Clock Distribution Networks, K. Jenkins, IBM TJ Watson Research Center, K. Shepard and Z. Xu, Columbia University

A circuit for on-chip measurement of period jitter and skew of clock distribution is described. The circuit uses a single latch and a voltage-controlled delay element. The circuit is evaluated in a stand-alone pad frame, where a jitter resolution of about 1 ps is demonstrated, and is incorporated in a 2 GHz clock distribution network to obtain on-chip period jitter and clock skew measurement.

9.7

4:50 pm

Mismatch-Tolerant Circuit for On-Chip Measurements of Data Jitter, K. Ichiyama, M. Ishida, T. Yamaguchi, Advantest Laboratories, and M. Soma, University of Washington

A new design for a mismatch-tolerant on-chip data jitter measurement circuit in 0.11- μ m CMOS is experimentally verified in this paper. It utilizes a data-to-clock converter, pulse generators, and an integrator followed by a sample-&-hold. The circuit's tolerance to data-rate changes is verified using 2.5 Gbps and 2.98 Gbps PRBS signals. The jitter gain of the prototype circuit is also shown to be less sensitive to variations in the supply voltage.

Session 10 – Panel Discussion

Oak Ballroom, Monday Afternoon, September 17
4:00 pm - 5:30 pm

**Are Analog Designers Hopeless At Scaling?
Will Digital Designers Eat Their Lunch At 45nm And Below?**

Organizer: Sudhir Aggarwal, Adonics Technology
Panel Moderator: Colin McAndrew, Freescale Semiconductor

Panelists:

Prof. Boris Murmann Stanford University	Dr. Ian Young Intel
Dr. Marcel Pelgrom NXP Semiconductor	Prof. Peter Kinget Columbia University
Prof. B.E. Boser University of California, Berkeley	Dr. Bill Krenik Texas Instruments

Three decades of relentless device scaling have resulted in reduction of the MOS transistor length to 45nm. Even shorter channel lengths are expected in the coming years. Scaling has provided consistent improvements in digital circuit density and performance. However, analog circuit designers have not been as successful in exploiting scaling for achieving improvement in performance or density. This raises a question as to what is limiting analog circuits scaling.

Is it limited by the nature of analog signal processing requirements? Or it may be that analog designers are hopeless at scaling. Can analog and digital system integration at and below 45nm? A panel consisting of experts will deliberate on the possible trends while providing insights into analog scaling.

Session 11 – Biomedical Sensors

Pine Ballroom, Monday Afternoon, September 17

Chair: Jackie Snyder

Co-Chair : Ken Szajda

This session presents innovative uses of integrated circuits for biomedical applications.

3:30 pm

Introduction

11.1

3:35 pm

A 0.18 μm CMOS Capacitive Detection Lab-on-Chip (INVITED PAPER), E. Ghafar-Zadeh and M. Sawan, Ecole Polytechnique de Montreal

In this paper, we put forward a CMOS-based capacitive interface circuit for Lab-on-Chip applications. This simple capacitive detector is implemented in the TSMC 0.18 CMOS process to which we incorporate microfluidic channels. In addition, we address the often-neglected challenges of microfluidic packaging for integrated biochemical sensors by proposing an efficient direct-write microfluidic packaging procedure. The simulation, fabrication and preliminary measurement results are also presented and discussed.

11.2

4:25 pm

A 400MHz RF Transceiver for Implantable Biomedical Micro-Stimulators, E. Lee, P. Hess, J. Gord, H. Stover and P. Nercessian, Alfred Mann Foundation

A 2.5MB/s, 400MHz RF transceiver was design for implantable biomedical micro-stimulators in a 0.18 μm CMOS process. It consists of a transmitter with an output power of -4.5dBm and a receiver that can detect input signal at $<-95\text{dBm}$. When one time slot of 6 μs in a $\sim 11\text{ms}$ data frame is used, the transceiver has an effective bit rate of 1.36kB/s, and consumes $\sim 23\mu\text{A}$ for receive and $\sim 8\mu\text{A}$ for transmit from a 3.6V battery. The total number of stimulators that the system can support is 852.

11.3

4:50 pm

A Monolithic Bandpass Amplifier for Neural Signal Processing with 25-Hz Low-Frequency Cutoff, P. Samsukha and S. Garverick, Case Western Reserve University

A monolithic bandpass amplifier for neural signal recording is reported. The low-frequency cutoff of the amplifier is obtained using low-gm feedback and a bias current of 500 pA to obtain a predictable response without off-chip components or calibration. The measured passband gain is 37.9 dB from 25 Hz to 15 kHz and input-referred noise is 1.04 μV rms, using a power consumption of 162 μW and a die area of 0.13 mm^2 in 0.5- μm CMOS.

11.4

5:15 pm

A Low Power Carbon Nanotube Chemical Sensor System, T. S. Cho, K.-J. Lee, J. Kong and A. Chandrakasan, Massachusetts Institute of Technology

This paper presents an energy efficient chemical sensor system that uses carbon nanotubes (CNT) as the sensor. The room-temperature operation of CNT sensors eliminates the need for micro hot-plate arrays, which enables the low energy operation of the system. The sensor interface chip is designed in a 0.18 μm CMOS process and consumes, at maximum, 32 $\mu\text{w};\text{W}$ at 1.83 kS/s conversion rate. The designed interface achieves 1.34% measurement accuracy over 10 k Ω - 9 M Ω dynamic range. The functionality of the full system, including CNT sensors, has been successfully demonstrated.

Poster Session

Cascade Ballroom, Monday, September 17

3:30 pm – 8:00 pm

(Authors are at the posters from 5:30 pm – 7:00 pm)

MP-01

A Re-configurable 0.5V to 1.2V, 10MS/s to 100MS/s, Low-Power 10b 0.13 μ m CMOS Pipeline ADC,
Y.-J. Kim, H.-C. Choi, S.-W. Yoo, S.-H. Lee, Sogang University, D.-Y. Chung, K.-H. Moon, H.-J. Park and J.-W. Kim, Samsung Electronics

This work describes a re-configurable 0.5V to 1.2V, 10MS/s to 100MS/s, 10b two-step pipeline ADC. The prototype ADC in a 0.13 μ m CMOS process demonstrates the measured DNL and INL within 0.35LSB and 0.49LSB, respectively. The ADC with an active die area of 0.98mm² shows the maximum SNDR and SFDR of 56.0dB and 69.6dB, respectively, and a power consumption of 19.2mW at a nominal condition of 0.8V and 60MS/s.

MP-02

20mW, 125 Msps, 10 bit Pipelined ADC in 65nm Standard Digital CMOS Process, *P. N. Singh, A. Kumar, C. Debnath and R. Malik, STMicroelectronics*

This paper describes a novel low power 10-bit 125Msps pipelined ADC implemented in 65nm standard digital CMOS process. Proposed ADC implements 2.5b/stage with amplifier shared between consecutive stages, achieves best in class FOM of 0.27pJ/step with conversion power of 0.16mW/Msps. The ADC amplifier employs novel techniques of adaptive biasing and cross coupled compensation to achieve improved settling behavior with significant power efficiency. ADC has 0.13mm² area and 9.26ENOB @125Msps dissipating 20mW power from 1.2v supply.

MP-03

A Low-Power, 6-bit Time-Interleaved SAR ADC Using OFDM Pilot Tone Calibration, *Y. Oh and B. Murmann, Stanford University*

A low-power analog-to-digital converter that exploits communication system resources for continuous self-calibration is presented. The proposed converter employs a time-interleaved array of successive approximation register ADCs. The inter-channel offset mismatches are adjusted by a calibration loop that utilizes the outputs of the FFT block of an orthogonal frequency division multiplexing (OFDM) receiver. The 6-bit prototype ADC, fabricated in a 0.18 μ m CMOS technology, achieves an SNDR of 35.4dB with a power consumption of 6.58mW at 200MS/s.

MP-04

A Fourth Order Elliptic Low-Pass Filter with Wide Range of Programmable Bandwidth, Using Four Identical Integrators, *B. Saeidi, Skyworks Solutions*

A new method to implement Elliptic filter with identical integrators and no derivatives is presented. Using identical capacitor arrays as opposed to highly spread capacitor arrays of conventional implementation makes Elliptic filter design with wide range of programmable/tunable bandwidths extremely simple, time-efficient and accurate. The proposed method also reduces the die size while realizing Elliptic filter more faithfully. To demonstrate the method, a fourth order Elliptic filter with nine programmable bandwidths ranging from 1.1MHz to 17.6MHz is designed. The 1.75mm² filter draws 10mA from 3.3V supply at output swing of 4.0Vppd in 0.35 μ m CMOS process to meet less than 50nV/Hz^{1/2} in-band output-referred noise and SFDR of better than 80dBc.

MP-05

An Idle-Tone Free Dynamic Element Matching Algorithm, M. Kepler and D. Thelen, AMI Semiconductor

This paper presents a first order noise shaped dynamic element matching (DEM) algorithm. The DEM algorithm was developed to improve the signal-to-noise and distortion ratio (SNDR) of a delta-sigma analog to digital converter (ADC). However, it can be applied to any system utilizing averaging and a plurality of unit components. Matlab simulations have shown that the presented algorithm eliminates idle-tones and provides almost a 30dB improvement in SNDR in a second order delta-sigma ADC.

MP-06

A 65-dB DR 1-MHz BW 110-MHz IF Bandpass Sigma-Delta Modulator Employing Electromechanical Loop Filter, R. Yu and Y. P. Xu, National University of Singapore

A 4th-order bandpass Sigma-Delta modulator employing electromechanical filter as loop filter is proposed. The electromechanical loop filter has the advantages of low power consumption and accurate center frequency without the need for tuning. The proposed bandpass Sigma-Delta modulator is implemented in a 0.35 μm SiGe BiCMOS technology and tested with a 110-MHz SAW filter. When sampled at 440MHz, the prototype chip achieves 65-dB DR and 60-dB peak SNDR in a 1-MHz signal bandwidth.

MP-07

A Current-mode ADC with Current Exchanging and Averaging Capabilities by Switching the Currents and Calculating Data in the Digital Domain, N. Yoshii, K. Mizutani and Y. Sugimoto, Chuo University

A 2 V, 25 MS/s, current-mode and pipelined analog-to-digital converter (ADC) which realizes a 1.5-bit bit-block architecture and uses a front-end current-mode sample-and-hold (S/H) circuit is described. The input and output currents in a current-mirror circuit are exchanged at every clock period to obtain the precise output current without suffering from poor current mismatch. The errors are canceled out by taking the average of the consecutive digital codes at the output part of the ADC.

MP-08

A 5-bit 4.2-GS/s Flash ADC in 0.13- μm CMOS, Y.-Z. Lin, Y.-T. Liu and S.-J. Chang, NCKU

A 5-bit flash ADC is fabricated in 0.13- μm CMOS process. Averaging and interpolation are discussed and analyzed for power reduction. This ADC consumes 180 mW from a 1.2 V supply and occupies 0.16 mm^2 area. Operating at 3.2 GS/s, the ENOB is 4.44 bit and ERBW 1.65 GHz. At 4.2 GS/s, the ENOB is 4.20 bit and ERBW 1.75 GHz. This ADC achieves FOMs of 2.51 and 2.80 pJ/conversion-step at 3.2 and 4.2 GS/s, respectively.

MP-09

A 1.2-V CMOS Limiter / RSSI / Demodulator for Low-IF FSK Receiver, Y.-C. Chen, Y.-C. Wu, P.-C. Huang, National Tsing Hua University

This paper presents low-voltage low-power limiter, RSSI, and demodulator designs for a low-IF wireless FSK receiver. The IF is located at 3MHz. The FSK demodulator is implemented by a delay-locked loop associated with the techniques of digital offset cancellation and modified phase-frequency detection. The demodulated data can be recovered with one-clock latency. The circuits in limiter and RSSI are all pseudo differential to minimize the requirement of the voltage headroom. Each gain cell with feedforward offset cancellation and common mode stabilization circuits can make sure its functionality against device mismatch. The chip uses a standard 0.18 μm CMOS process. The active area is 0.11 mm^2 . With a single 1.2-V power supply, measurement results show that the 55dB gain, 15MHz bandwidth limiter and the RSSI consume 1.9mA. The FSK demodulator part consumes 300 μA .

MP-10

Temperature Sensor Design in a High Volume Manufacturing 65nm CMOS Digital Process, D. Duarte, G. Geannopoulos, U. Mughal, K. Wong and G. Taylor, Intel Corporation

Thermal management (TM) allows the system architect to design a cooling solution based on real-life power consumption, not peak power. The on-die thermal sensor circuit, as the core of the TM system, monitors the on-die junction temperature (T_j). We present a novel high-linearity thermal sensor topology with built-in circuit support for correction of systematic shifts in the transfer function correction. Results obtained on the 65nm Pentium®4 Processor demonstrate the feasibility and effectiveness of the design.

MP-11

Six and Seven Transistor Leakage Suppressed SRAM Cells with Improved Read Stability, S. Badrudduza and L. Clark, Arizona State University

Static random access memories with six and seven transistor cells that maintain full static noise margin during read operation and reside in low leakage voltage collapsed state when unselected are presented. The memory test circuits are fabricated on a 0.13 μm CMOS process technology. The cells are 11% larger than a conventional SRAM cell. Measured test results verify the power, speed and usable range of power supply voltages for the designs.

MP-12

Rapid Estimation of the Probability of SRAM Failure due to MOS Threshold Variations., S. Srivastava and J. Roychowdhury, University of Minnesota

Accurate estimation of the effects of threshold variations, in particular yield loss, is crucial during the design of robust SRAM cells and memory arrays in deep submicron technologies. We present an efficient technique to calculate yield loss due to access-time, static noise margin, etc, related failures. Our method does not rely on Monte-Carlo techniques; instead, it finds the boundary in V_t (threshold voltage) parameter space between success and failure regions and uses quick geometrical calculations to find the yield. The V_t boundary curve is found efficiently via an Euler-Newton curve tracing technique, adapted from mixed-signal/RF simulation, that guides detailed SPICE-level simulation with accurate MOS device models. We compare and validate the new method against Monte-Carlo style yield estimation, obtaining superior accuracies and speedups of more than 10 x.

MP-13

A Stable SRAM Mitigating Cell-Margin Asymmetry with A Disturb-Free Biasing Scheme, T. Suzuki, K. Satomi and H. Akamatsu, Matsushita Electric Industrial Co., and H. Yamauchi, Fukuoka Institute of Technology

A Reduced-Vt SRAM (LVt) cell and a unique disturb-free biasing scheme have been proposed for the low-voltage application. The proposed LVt cell mitigated the cell-margin asymmetry and improved the SNM at high z-score range up to 7σ random-Vt fluctuation at the cell-bias=0.5V. Another unique disturb-free biasing scheme canceled the substantial trade-off relationship between the cell-margins. The cell/logic bias voltage were reduced to 0.5/0.7V with higher stability over 6σ Vt fluctuation compared with the conventional biasing scheme. The operating current was reduced by 31%.

MP-14

Dynamic Data Stability in Low-power SRAM Design, M. Sharifkhani, S. Jahinuzzaman and M. Sachdev, University of Waterloo

SRAM cell stability measurement is traditionally based on 'static criteria' of data stability requiring 3 coincident points in butterfly curves. We introduce 'dynamic criteria' of stability. This enables reducing cell operating voltage without compromising reliability once cell access-time is less than cell time-constant. Experimental results of a 40Kb SRAM exploit the dynamic criteria, offering 6 times smaller area overhead compared to recent subthreshold schemes. The SRAM unit realized in 0.13 μm -CMOS consumes 702uW at 100MHz during write-operation and offers a 27pA/cell leakage.

MP-15

An 8T Subthreshold SRAM Cell Utilizing Reverse Short Channel Effect for Write Margin and Read Performance Improvement, T.-H. Kim, J. Liu and C. H. Kim, University of Minnesota

We propose a technique for improving write margin and read performance of 8T subthreshold SRAMs by using long channel devices to utilize the pronounced reverse short channel effect. Simulations show that the proposed cell at 0.2V has a write margin equivalent to a conventional cell at 0.27V. The Ion-to-Ioff ratio of the read path also improved from 169 to 271 and a 52% speedup for read was achieved. The cell area overhead was 20%.

MP-16

Solution to ESD Induced Pocket Isolation Failure in Multi Well CMOS, T. Ruud, B. Rasmussen, B. Greenwood, and M. Tyler AMIS

An N+ pocket isolation weakness was identified during ESD qualification of a multi-well CMOS process. Upon initial process ESD qualification, inter-domain testing identified leakage failures in unstressed power supply domains. This work describes how novel failure analysis techniques identified a parasitic NPN that was instrumental in creating this unusual failure signature. Strategic changes to and placement of ESD protection elements and improved metalization successfully prevented activation of parasitic bi-polar transistors hence, avoiding expensive process modifications.

MP-17

Integration of CMP Modeling in RC Extraction and Timing Flow, H. Liao, R. Radojcic, Qualcomm, L. Song, N. Jakatdar, Cadence Designs

As technology scaling progresses into 65nm and below nodes, on chip variation due to Chemical Mechanical Polishing (CMP) becomes relatively larger and needs to be considered. In this paper, we demonstrate that by incorporating CMP model in the post layout RC extraction flow, the thickness variations are reflected more accurately and the capacitance value extracted are different from results obtained using the polynomial equation. As a result, new timing violations are detected with CMP modeling.

MP-18

Integrated Inductor Actively Engaging Metal Filling Rules, J.I. Kim, B. Jung, D. Peroulis, Purdue University, D. Kim, J. Kim, C. Cho, IBM

This paper reports a new strip-patterned integrated inductor that actively engages metal filling rules leading to reduced manufacturing cost and process-induced uncertainties while simultaneously maintaining state-of-the-art performance. The striped inductor consists of parallel horse shoe-shape metal lines in the foot print of a single-line inductor. The new inductor structure is backed by experimental and simulated results that demonstrate the design methodology in the presence of process uncertainties typically not known to the circuit designer.

MP-19

A Wide Range Spatial Frequency Analysis of Intra-Die Variations with 4-mm 4000 x 1 Transistor Arrays in 90nm CMOS, D. Levacq, T. Minakawa, M. Takamiya and T. Sakurai, University of Tokyo

In order to investigate the systematic intra-die variations, the intra-die threshold voltage and on-current variations are measured thanks to 4-mm 4000 x 1 transistor arrays with 1 μm transistor-pitch in a 90nm CMOS technology, achieving the widest spatial distribution range. The spatial frequency analysis of the variations indicates that both variations are random across 4 mm.

MP-20

Architecture of Via Programmable Logic using Exclusive-OR Array (VPEX) for EB Direct Writing, A. Nakamura, M. Kawaharazaki, T. Fujino, Ritsumeikan University, M. Yoshikawa, Meijo University

We propose the novel architecture of Via Configurable Logic Device called VPEX which is optimized for Electron Beam direct writing. The logic element of VPEX consists of complex gate type EXOR and INV. This element can output 12 logics by changing via1 layout. The speed performance of VPEX is 1.5 times slower than ASICs but much higher than FPGAs. We believe that VPEX with EB is the best solution for low-volume production LSIs.

MP-21

Receiver Offset Cancellation in 90-nm PLD Integrated SERDES, S. Maangat, T. Nguyen, W. Wong, S. Shumarayev, T. Tran, T. Hoang and R. Cliff, Altera Corporation

A wide-range transceiver was designed and fabricated in a 90-nm TSMC CMOS logic process. Each transceiver channel contains Clock Data Recovery (CDR) circuit. Voltage offsets in the receive path degrade the performance of the CDR by reducing the precision of bit detection and cause duty cycle distortion. Presented in this paper is a methodology to cancel voltage offsets in the receive path with a soft intellectual property (IP) core programmed in the PLD.

MP-22

Dual True Random Number Generators for Cryptographic Applications Embedded on a 200 Million Device Dual CPU SoC, V. von Kaenel and T. Takayanagi, PASEmi

Implementations of a thermal noise and a chaotic True Random Number Generator are presented. They are embedded in a large commercial SoC. Their outputs are combined to improve the randomness of the bit stream. The design goal was to minimize the effect of data dependent noise injected by the supplies and substrate. The random bit rate is 2Mbit/s and passes the DIEHARD test suite. The circuit area is 0.21mm^2 in a 65nm CMOS process.

MP-23

A 0.22nJ/b/iter 0.13 μm Turbo Decoder Chip Using Inter-Block Permutation Interleaver, C.-C. Wong, C.-H. Tang, M.-W. Lai, Y.-X. Zheng, C.-C. Lin, H.-C. Chang, C.-Y. Lee and Y.-T. Su, National Chiao Tung University

This paper presents a high speed turbo decoder containing 32 MAP decoders with an inter-block permutation interleaver. This network guarantees contention-free property and promise parallel processing of turbo decoder without performance degradation. In addition, our approach also features a relocated radix-2² ACS structure to reduce the critical path delay. After manufacturing by 0.13 μm CMOS process, the test results show the energy efficiency is 0.22nJ/b/iter in the 160Mb/s data rate.

MP-24

A 10-Gb/s CMOS Serial-Link Receiver using Eye-Opening Monitoring for Adaptive Equalization and for Clock and Data Recovery, T. Suttorp and U. Langmann, Ruhr-Universität Bochum

A 10-Gb/s receiver for chip-to-chip communication is presented which employs an eye-opening monitor for both adaptive equalization and digital clock and data recovery (CDR). The prototype circuit fabricated in 0.13- μm CMOS technology consumes about 164 mW at 1.2 V supply voltage and occupies about $0.39 \times 0.39 \text{mm}^2$. The CDR fulfills the SONET/SDH jitter tolerance requirements at a $2^{31}-1$ PRBS and a BER of $< 10\text{E}^{-12}$. Successful adaptive equalization for FR4 channels up to 76 cm is also demonstrated.

MP-25

A 1-V, 1.4–2.5 GHz Charge-Pump-Less PLL for a Phase Interpolator Based CDR, J. Park, Samsung Electronics, J. F. Liu, C. P. Yue, University of California, L. R. Carley, Carnegie Mellon University

A 1.4-2.5 GHz charge-pump-less phase locked loop and a linear phase interpolator with dummy cells to enhance linearity are implemented in 0.13- μm CMOS. The loop filter with RC integrators and a V-I converter are proposed for achieving wide frequency range and high linearity in the voltage controlled oscillator under a low supply voltage. The measured RMS and peak-peak jitters are 4.05 ps and 28.18 ps at 2 GHz, respectively. The measured DNL and INL of the PI are 0.27 LSB and 0.68 LSB, respectively.

MP-26

A 10Gb/s Equalizer with Decision Feedback for High Speed Serial Links, A. Kiaei, A. Bahai, T. Lee, Stanford University and B. Matinpour, National Semiconductor

A 10Gb/s equalizer using both feedforward and decision-feedback equalization is designed for high speed serial-links. The chip is implemented in a standard 0.25 μ m SiGe BiCMOS technology with 50 GHz peak ft, and packaged in a commercial LLP package. Using a 4-stage feedforward and 2-tap post-cursor cancellation, this equalizer achieves a total peak-to-peak jitter of 27ps and 33ps for 10" and 20" of copper traces on FR4, respectively. The transmitter uses NRZ signaling with no pre-emphasis.

MP-27

Concurrent Digital Adaptive Decision Feedback Equalizer for 10GBase-LX4 Ethernet System, C.-S. Lin, Y.-C. Lin, M.-T. Shiou, National Central University and S.-J. Jou, National Chiao Tung University

An all digital 3.5Gbps blind Adaptive Decision Feedback Equalizer (ADFE) is designed for 10GBase-LX4 IEEE 802.3ae standard. It uses 5 parallel equalization blocks each with 6 taps and 4 taps for each Feed-Forward Equalizer (FFE) and Feed-Back Equalizer (FBE). This concurrent ADFE has core area of 0.864 \times 0.864 mm² with operation up to 3.5 Gbps using 1.2-V supply in a 0.13 μ m CMOS process.

MP-28

A 2.5 Gbps CMOS Fully Integrated Optical Receiver with Lateral PIN Detector, W.-Z. Chen and S.-H. Huang, National Chiao Tung University

This paper presents the design of a monolithically integrated CMOS optical receiver, including a photo detector, a transimpedance amplifier, and a post limiting amplifier on a single chip. A novel PIN detector is proposed and adopted in this design without technology modification. The optical receiver is capable of delivering 420 mVpp to 50 ohm output load and operating up to 2.5 Gbps without an equalizer. Implemented in a generic 0.18 μ m CMOS technology, the total power dissipation is 138 mW. The chip size is 0.53 mm².

MP-29

A New Spread Spectrum Clock Generator for SATA Using Double Modulation Schemes, Y.-B. Hsieh, National Chiao Tung University and Y.-H. Kao, Chung Hua University

A new spread spectrum clock generator (SSCG) using double modulation is presented in this paper. Not only the divider is varied, but also the voltage controlled oscillator is modulated. This technique can enhance the modulation bandwidth so that the effect of EMI suppression is improved and can optimize the jitter caused by the sigma-delta modulator. In addition, the method of two-path is applied to reduce the capacitance value such that the total integration can be achieved. The proposed SSCG has been fabricated in a 0.18 μ m CMOS process. The clock of 1.5GHz with down spread ratio of 0.5% is realized for applications to serial ATA. The 19.63dB EMI reduction (RBW=10KHz) and 35ps-pp period jitter are achieved in this study. The size of chip area is 0.44 \times 0.48mm². The power consumption is 27mW.

MP-30

An Energy-efficient Multi-bit Quaternary Current-mode Signaling for On-chip Interconnects, V. Venkatraman and W. Burlison, University of Massachusetts Amherst

We present a multi-bit quaternary current-mode signaling (MQCMS) system which transmits two digital signals over one interconnect using current levels and is implemented on a 130nm IBM CMOS process. Measurement results show the MQCMS system with data rates of 2.3Gb/s/ch to 1.1GB/s/ch and energy of 0.19pJ/b to 0.57pJ/b for wires between 1mm to 5mm respectively. Measurement results also show 2x reduction in energy per bit compared to repeaters for a 5mm wire. Overall, MQCMS provides an energy-efficient, crosstalk noise resilient, on-chip interconnect signaling system with data rates comparable to conventional repeaters.

MP-31

A 0.6GHz to 2GHz Digital PLL with Wide Tracking Range, V. Kratyuk, P. K. Hanumolu, K. Mayaram and U.-K. Moon, Oregon State University

A digital PLL employing an adaptive tracking technique and a novel frequency acquisition scheme achieves a wide tracking range and fast frequency acquisition. The test chip fabricated in a 0.13 μ m CMOS process operates from 0.6GHz to 2GHz and achieves better than ± 3200 ppm frequency tracking range when the reference clock is modulated with a 1MHz sine wave.

MP-32

A 1V, 1mW, 4GHz Injection-Locked Oscillator for High Performance Clocking, L. Zhang, B. Ciftcioglu and H. Wu, University of Rochester

A new injection-locked oscillator was designed for high performance clocking purpose. It uses transformer injection and incorporates a switched capacitor array for digital delay tuning. A 4GHz test chip was implemented in 0.18 μ m CMOS with four ILOs driven by an H-tree. 5-bit digital deskew achieves 55ps delay tuning range and 1.8ps resolution. Measurement shows that only 30fs cycle-to-cycle jitter degradation was introduced and no phase noise degradation at frequency offset up to 600kHz.

Session 12 – Nyquist A/D Converters

Oak Ballroom, Tuesday Morning, September 18

Chair: George La Rue

Co-Chair : Yusuf Haque

The first four papers present pipelined A/D converters with resolution of 10 to 14 bits and conversion rates below 210 MS/s. These are followed by higher conversion rate circuits up to 4 GS/s.

8:25 am

Introduction

12.1

8:30 am

A 14-b 30MS/s 0.75mm² Pipelined ADC with On-Chip Digital Self-Calibration, H.-Y. Lee, T.-H. Oh, H.-J. Park, J.-W. Kim, Samsung Electronics, H.-S. Lee, M. Spaeth, Massachusetts Institute of Technology

A 14-b 30MS/s CMOS pipelined ADC is presented. To facilitate digital calibration, a simple 1-b per stage architecture with redundancy is used. The ADC fully integrates digital self-calibration, which performs overall sequence by one flag signal. Implemented in a 90nm digital CMOS process, the prototype ADC achieves 83.7dB SFDR and 69.3dB SNDR with calibration. Its active area is 0.75mm² including the on-chip calibration logic and the total power consumes 106mW with 3.3V and 1.0V supply.

12.2

8:55 am

A 1.8V 10b 210MS/s CMOS Pipelined ADC Featuring 86dB SFDR without Calibration, J. Li, R. Leboeuf, M. Courcy and G. Manganaro, National Semiconductor Corporation

A 1.8V 10b 210MS/s CMOS pipelined ADC in 0.18 μ m CMOS process is presented. The low power consumption at high sampling rate is achieved by using an opamp-sharing technique in 2.5b/stage pipelined ADC architecture. The opamp settling behavior is well controlled through a regulated switch driving scheme. With a 20MHz input signal, the ADC achieves 85.9dB SFDR and 9.57ENOB at 210MS/s. Better than 76dB SFDR and 9.5ENOB performance is maintained for input frequency up to 100MHz. The ADC consumes 140mW at 1.8V. The die area is about 1.5mm².

12.3

9:20 am

Low-Power and High-Speed Pipelined ADC Using Time-Aligned CDS Technique, Y.-J. Kook, U.-K. Moon, Oregon State University and J. Li, B. Lee National Semiconductor

Time-aligned Correlated Double Sampling (CDS) technique, which overcomes the error accumulation problem found in the time-shifted CDS technique [4], is proposed. This technique allows low gain opamp based switched-capacitor operation to achieve the equivalent accuracy that is traditionally possible only in high gain opamp based switched-capacitor operation. This allows simple single stage opamps to be used, leading to low-power and high-speed performance. As a proof of concept, a prototype pipelined analog-to-digital converter (ADC) is fabricated in a 0.18 μ m CMOS process. Measured results demonstrate 1.8V 10b 100MS/s 50mW ADC.

12.4

9:45 am

A 1V 10b 30MSPS Switched-RC Pipelined ADC, G.-C. Ahn, M.G. Kim, P. Hanumolu and U.-K. Moon, Oregon State University

A 10b 30MS/s pipelined ADC using fully-differential switched-RC multiplying digital-to-analog converter (MDAC) is presented. It utilizes a resistive loop to reset the feedback capacitor in the MDAC without using the floating switch. The measured differential and integral nonlinearities of the prototype IC fabricated in a 0.13 μ m MOS process are less than 0.54 LSB and 1.75 LSB respectively. The prototype ADC achieves 51.6dB SNDR and 65.9dB SFDR with 1V supply while consuming 17mW power.

10:10 am - Break

12.5

10:25 am

A Time-Interleaved Track & Hold in 0.13 μ m CMOS sub-sampling a 4 GHz Signal with 43dB SNDR, S. Louwsma, E. van Tuijl, B. Nauta, University of Twente, and M. Vertregt, NXP Semiconductor

A 16-channel time-interleaved Track and Hold is presented. Three techniques are introduced enabling a high bandwidth and linearity and good timing alignment. Integrated ADCs are used to evaluate the performance of the T/H. Single channel performance is 43 dB SNDR at an input frequency of 4 GHz. Multi-channel performance is 48 dB SNDR at 1.35 GS/s with an ERBW of 1 GHz. The power consumption of the T/H including clock-driver and buffers is 74 mW.

12.6

10:50 am

A 43mW Single-Channel 4GS/s 4-Bit Flash ADC in 0.18 μ m CMOS, S. Sheikhaei, S. Mirabbasi and A. Ivanov, University of British Columbia

A low-power small-area single-channel 4GS/s 4-bit flash ADC in 0.18 μ m CMOS is presented. The entire ADC is implemented using CML blocks. To enhance the speed, both analog (comparators) and digital (encoder) parts of the ADC are fully pipelined. Furthermore, a reformulation for the encoder logic functions is introduced to reduce the wiring delay in the layout. The ADC achieves a figure of merit of 2.14pJ/conversion-step. The ADC area including the resistor ladder is 0.06mm² and the power consumption is 43mW when supplied with 1.8V.

12.7

11:15 am

A 57dB SFDR Digitally Calibrated 500MS/s Folding ADC in 0.18 μ m Digital CMOS, I. Bogue and M. Flynn, University of Michigan

A digitally calibrated 8-bit folding ADC incorporating redundancy and reassignment is described. Small, redundant folder and comparator circuits generate 1024 available zero-crossings. An entirely self-

contained calibration engine selects 255 zero-crossings from the available set. Unselected circuits are powered down. The calibration breaks the link between ADC performance and analog accuracy, allowing small transistors to be used in the signal path. Fabricated in 0.18 μm digital CMOS, the DNL of the uncalibrated ADC is 6.7LSB and 0.8LSB, before and after calibration, respectively. SFDR remains above 55dB up to a sampling rate of 550MS/s. The total die area is 1.2mm².

12.8

11:40 am

A Sample-Time Error Compensation Technique for Time-Interleaved ADC Systems, A.

Haftbaradaran and K. W. Martin, University of Toronto

Sample-time error among different channels of a time-interleaved Analog-to-Digital Converter (ADC) is a factor in significant degradation of the ADC performance, especially in high frequencies. A two-channel, time-interleaved ADC structure with a background sample-time error compensation technique has been implemented. The sample-time error detection technique uses random data and has been implemented in the digital domain at a low level of complexity. The error correction is performed by adjusting the delay of the clock path of one channel, using a 6-bit Digitally-Controlled Delay Element (DCDE). At a sampling rate of 400 MSamples/s, the experimental results show that the Spurious-Free Dynamic Range (SFDR) of the ADC system is improved to 58.8 dB at 190 MHz. The ADC system achieves a Signal-to-Noise-and-Distortion Ratio (SNDR) of 59.6 dB at 5 MHz and 55.2 dB at 190 MHz after compensation. This error compensation method is especially suitable for time-interleaved ADCs used in digital data communication systems.

Session 13 – Clocking and CDRs

Fir Ballroom, Tuesday Morning, September 18

Chair : Jafar Savoj

Co-Chair: Kimo Tam

This session explores modern clocking techniques with an emphasis on digital enhancement along with new CDR implementations.

8:25 am

Introduction

13.1

8:30 am

Low-Jitter and Large-EMI-Reduction Spread-Spectrum Clock Generator with Auto-Calibration for Serial-ATA Application, T. Kawamoto, Hitachi Ltd., T. Takahashi, H. Inada and T. Noto, Renesas

Technology

A low jitter VCO with high-frequency-limiter and an auto-calibration technique was developed for a spread-spectrum clock generator (SSCG) by using a 0.13- μm CMOS process for Serial-ATA applications. The limiter prevents the SSCG from going into an unlocked state, and the auto-calibration technique optimizes the performance by controlling VCO gain and maximum output frequency. Rms-jitter variation at 1.5 GHz is improved from 2.1-7.8 ps to 1.9-3.3 ps and the EMI reduction of 10.0 dB is achieved.

13.2

8:55 am

Wide Lock-Range, Low Phase-Noise PLL using Interpolative Ring-VCO with Coarse Frequency Tuning and Frequency Linearization, H. Kodama, H. Okada, H. Ishikawa and A. Tanaka, NEC

Corporation

To relax the trade-off relationship between tuning range and phase noise, we have developed a new interpolative ring-VCO having a wide control voltage range over which frequency variation is linear. A wide lock-range, low phase noise PLL incorporating this VCO has been fabricated in a 90 nm CMOS process. It successfully offers between 3.432–4.488 and 6.600–9.240 GHz, as well as low integrated phase noise, less than 4 degrees.

13.3

9:20 am

A 3.2Gb/s Oversampling CDR with Improved Jitter Tolerance, M. Brownlee, P. Hanumolu and U.-K. Moon, Oregon State University

A 3.2Gbps CDR circuit employs an oversampling architecture to decouple the tradeoff between jitter generation and jitter tolerance. The test chip fabricated in a 0.13 μ m CMOS process achieves a 30x increase in the jitter tolerance corner without increasing recovered clock jitter. Power consumption is 19.5mW from a 1.4V supply at 3.2Gbps and die area is 0.081mm².

13.4

9:45 am

A 2.5Gb/s Burst-Mode CDR based on a 1/8th Rate Dual Pulse Ring Oscillator, S. Gierkink, Conexant

A 2.5Gb/s burst-mode CDR uses a 1/8th rate ring oscillator with two phase independent pulses running simultaneously. One pulse sets the ring delay by phase locking it to a reference, the other tracks the data. Phase acquisition is instantaneous. CID tolerance is > 72 bits. The 0.6mm² 0.13 μ m CMOS chip includes a CML input buffer, PLL, PRBS checker and 1:8 demux. It has 2.7UIpp jitter tolerance at 100kHz and consumes 42mW from a 1.2V supply.

10:10 am - Break

13.5

10:25 am

Digitally-Enhanced Phase-Locking Circuits (INVITED PAPER), P. Hanumolu, U.-K. Moon and K. Mayaram, Oregon State University, G.-Y. Wei, Harvard University

In this paper, we present an overview of digital techniques that can overcome the drawbacks of analog phase-locked loops (PLLs) implemented in deep-submicron CMOS processes. The design of key building blocks of digital PLLs such as the time-to-digital converter and digital-to-frequency converters are discussed in detail. The implementation and measured results of two digital PLL architectures, (1) based on a digitally controlled oscillator and (2) based on a digital phase accumulator, are presented. The experimental results demonstrate the feasibility of using digital PLLs in digital systems requiring high-performance PLLs.

13.6

11:15 am

A Low-Jitter Open-Loop All-Digital Clock Generator with 2 Cycle Lock-Time, M.-Y. Kim, D. Shin, H. Chae, S. Ok and C. Kim, Korea University

A portable multiphase clock generator, independent of input duty ratio, has been developed. The proposed open-loop and full-digital architecture has a fast lock time of two clock cycles and is a simple, robust and portable IP. In addition, the complementary delay line is implemented to achieve high phase resolution at a wide frequency range. The generator has been implemented in a 0.18 μ m CMOS process and operates at variable input frequencies ranging from 800MHz to 1.6GHz.

13.7

11:40 am

An All-Digital 90-Degree Phase-Shift DLL with Loop-Embedded DCC for 1.6Gbps DDR Interface, J.-H. Bae, J.-Y. Sim, H.-J. Park, POSTECH and J.-H. Seo, H.-S. Yeo, J.-W. Kim, Samsung Electronics

An all-digital 90° phase-shift DLL is proposed for 1.6Gbps DDR interface by using a loop-embedded DCC and a binary phase detector with the lock range extended to $0\sim 4\pi$ radians. The DCC has a small delay and the fixed rising-edge property for loop-embedding. The chip fabricated with a 0.13 μ m CMOS process gives the DLL data rate of 667Mbps~1.6Gbps and the output duty cycle of 47.8%~49% for the input duty cycle of 23%~76%, at 1.6Gbps and 1.2V.

Session 14 – Power Management Techniques

Pine Ballroom, Tuesday Morning, September 18

Chair: Steve Garverick

Co-Chair: Makoto Takamiya

This session addresses issues in power management, including ac-dc and dc-dc converters, regulators, controllers, timers, and low-power drivers.

8:25 am

Introduction

14.1

8:30 am

A Low Noise Buck Converter with a Fully Integrated Continuous Time Sigma Delta Modulated Feedback Controller, M. Wong, Freescale Semiconductors, B. Bakkaloglu and S. Kiaei, ASU

A low noise synchronous buck converter with a fully integrated second order single-bit continuous time sigma delta modulator (CT-sigma delta M) based controller is presented. The converter is designed and fabricated on a 0.18 μ m SiGe process. The feedback CT-sigma delta M is sampled at 10MHz with a single-bit non-return-to-zero (NRZ) output. Compared to a traditional PWM controller, the CT-sigma delta M controlled converter shapes the out-of-band noise and suppresses the in-band noise at the switching node by 25dB with 92% efficiency.

14.2

8:55 am

A Compact Pulse-Based Charge Pump in 0.13 μ m CMOS, J. Holleman, B. Otis and C. Diorio, University of Washington

In this paper, we present a new class of charge pump capable of generating voltages 3.75 times greater than the supply in a single clock cycle. It occupies .005 mm² in a 0.13 μ m CMOS process and can operate with a supply voltage between 0.4V and 1.2V, or as low as 0.2V with some pulse-shape distortion. Our charge pump can provide output voltages of up to 3.9V with less than 10nW of standby power dissipation.

14.3

9:20 am

An Efficiency-Enhanced Integrated CMOS Rectifier with Comparator-Controlled Switches for Transcutaneous Powered Implants, S. Guo and H. Lee, University of Texas

This paper presents a high-efficient rectifier for high-current transcutaneous power transmission in biomedical implants. By using comparators to control power nMOS transistors functioning as switches with unidirectional current flow, the rectifier dropout voltage is decreased to improve the power efficiency. The unbalanced biasing scheme in the comparator also minimizes the reverse leakage current. Implemented in a standard 0.35 μ m CMOS, the rectifier operates at 1.5MHz, achieves the peak conversion ratio of 95% and can deliver up to 20mA output current.

14.4

9:45 am

Integrated Regulation for Energy-Efficient Digital Circuits, E. Alon, University of California Berkeley, and M. Horowitz, Stanford University

Linear regulation can reduce the effective supply impedance of digital circuits without increasing their total power dissipation. This can be achieved with a push-pull regulator topology that uses a second, higher-than-nominal supply, comparator-based feedback, and a switched-source follower output stage. Measured results from a 65nm SOI test-chip verify that by using these techniques, regulation reduces supply noise by ~30% while also enabling a slight decrease (~1.4%) in total power.

10:10 am – Break

14.5

10:25 am

An EEPROM Programming Controller for Passive UHF RFID Transponders with Gated Clock Regulation Loop and Current Surge Control, R. Barnett, Texas Instruments, and J. Liu, University of Texas Dallas

This paper describes an EEPROM programming controller for a RFID IC. A gated clock regulation loop is proposed to regulate the programming voltage over a wide range of RF input power. A current surge limiting architecture prevents a collapse of the rectified supply during startup of the charge pump and a switched bandgap reference is proposed for reducing power and area. The 0.35 μ m CMOS IC provides 14V from a 2V rectified supply and consumes 7 μ W.

14.6

10:50 am

A Sub-pW Timer Using Gate Leakage for Ultra Low-Power Sub-Hz Monitoring Systems, Y.-S. Lin, D. Sylvester and D. Blaauw, University of Michigan

In this work, we presented a novel ultra low power timer designed using the gate leakage of MOS capacitors. The test chip was fabricated with 0.13 μ m CMOS technology with area of 480 μ m². Measurement results show that the circuit functions correctly at a wide range of supply voltage from 300mV to 1.2V. The temperature sensitivity is 0.16%/°C at 600mV and 0.6%/°C at 300mV. The power dissipation is less than 1pW running at 20C and 300mV.

14.7

11:15 am

CMOS-Based MEMS Mirror Driver for Maskless Lithography Systems, J. Lee, J. Weiner, Y. Baeyens, V. Aksyuk, Y.-K. Chen, Alcatel-Lucent, H.-H. Chen, Mediatek

This paper presents a low-power MEMS mirror driver for maskless lithography systems. The CMOS driver consists of a 512x128 analog memory cell array to drive the position of 512x128 MEMS mirror array. The row driver employs an analog de-multiplexing architecture, which eliminates the need for precise matching among multiple row driver characteristics. It uses two parallel high-speed 8-b DACs with 128 sample-and-hold amplifiers (SHAs) to write a multilevel data into memory cells. The driver chip is implemented in a 0.35 μ m digital CMOS process. It consumes a 120mA power with 3/3.6 V supplies.

Session 15 – CMOS Scaling and Technology Implications

Cedar Ballroom, Tuesday Morning, September 18

Chair: David Sunderland

Co-Chair: Jordan Lai

This session of invited papers addresses important issues related to maintaining Moore's Law scaling beyond 45nm, focusing on device technology, package technology, reliability and physical analysis.

8:25 am

Introduction

15.1

8:30 am

Reliability Trends with Advanced CMOS Scaling and the Implications for Design (INVITED PAPER), J. McPherson, Texas Instruments

Scaling has pushed existing CMOS materials much closer to their intrinsic reliability limits. With the expected introduction of new materials (metal gate electrodes, high-k gate dielectrics, strained silicon, and ultra-low interconnect dielectrics) legacy-based design rules should be challenged as to their validity when designing with these new materials. This work will focus on several key reliability issues: TDDB, NBTI, HCI, Electromigration, and Stress Migration as we continue to scale with the new materials.

15.2

9:20 am

Evolution of CMOS Technology at 32 nm and Beyond (INVITED PAPER), G. Shahidi, IBM

Over the last 15 years, there has been a new CMOS technology node approximately every two years. The key feature of every node has been 2X density shrink and ~35% performance gain per technology node. Chip power has been increasing rapidly, approaching air cool limit. Power limit is transforming CMOS scaling to more of a density driver. As we move to 32 nm node and beyond a number of additional fundamental challenges are faced, which may force additional rethinking of how scaling has been done. This paper is an overview of some upcoming challenges and possible ways of addressing them.

15.3

9:45 am

High-K/Metal Gate Technology: A New Horizon (INVITED PAPER), M. Khare, IBM

High-K/Metal Gate technology represents a fundamental change in transistor structure that restarts gate length scaling, enables performance improvement and offers chip power reduction. The gate stack presented is compatible with conventional high temperature CMOS processing and existing performance enhancement elements. A new knob in the form of metal gate work function promises separate and better optimization for High Performance and Low Power applications. This technology introduces a unique PBTI reliability mechanism for N-FET that is now well understood and modeled.

10:10 am - Break

15.4

10:25 am

Revolutionary NanoSilicon Ancillary Technologies for Ultimate-Performance Gigascale Systems (INVITED PAPER), M. Bakir, B. Dang and J. Meindl, Georgia Institute of Technology

This paper describes electrical, optical, and fluidic (or 'trimodal') chip I/O interconnect networks for gigascale systems to meet and exceed end-of-roadmap projections in the areas of power delivery, off-chip bandwidth, and heat removal, respectively. The trimodal I/O technology is proposed to overcome the adverse effects of conventional silicon ancillary technologies on the performance of a gigascale system. We describe trimodal I/O interconnect configurations, fabrication, assembly, and testing.

15.5

11:15 am

Reverse Engineering in the Semiconductor Industry (INVITED PAPER), R. Torrance and D. James, Chipworks, Inc.

This paper covers the place of reverse engineering in the semiconductor industry, and the techniques used to obtain information from semiconductor products. The paper covers product teardowns; system-level analysis, both hardware and software; circuit extraction, from the transistor level up; and process analysis, looking at how a chip is made, and what it is made of. Examples are also given of each type of reverse engineering.

CICC Luncheon

Sierra Ballroom, Tuesday, September 18
12:00 – 1:30 pm

12:00 pm

Seating for Lunch

12:35 pm

Welcome and Introduction of Speaker

Ann Marie Rincon, Conference Chair

12:40 pm

Luncheon Presentation: Growing Up with Wires and Batteries, Paul Brokaw, Analog Devices

In a time when a computer was a mechanical adding machine, with a crank like a one-armed bandit turned to tally keyed in figures, kids could take things apart and see how they worked. What passed for electric circuits often consisted of things like lights or bells wired together and powered by batteries.

This talk will be a series of recollections from the days of electric telephones and vacuum tubes, to beyond the invention of the transistor. It will be a mixture of the technology and a few of the characters that have had a great influence on my life.

Mr. Brokaw holds a BS in Physics from Oklahoma State University. He has worked for Wells Surveys Inc, Authur D. Little Inc., Communication Technology Inc., Nova Devices, and Analog Devices where he is currently an Analog Fellow. He has designed a variety of products and holds upward of 100 U.S patents in areas including monolithic A/D and D/A converters, sensors, voltage references, amplifiers, power management circuits, and ASICs. He was selected in 1993 as "Innovator of the Year" by the readers of EDN magazine and more recently elected to the Electronic Design Magazine "Hall of Fame." Over his career he has presented and published papers at numerous technical conferences and in IEEE journals, served as guest editor of the JSSC, and is a life fellow of the IEEE.

1:20 pm

Introduction of the Technical Program Chair for CICC 2008, Ann Rincon, Conference Chair

Session 16 – Signal and Data Processing

Oak Ballroom, Tuesday Afternoon, September 18

Chair: Charles Thomas

Co-Chair: Ram Krishnamurthy

This session explores new signal and data processing integrated circuits for a diverse range of applications including medical devices, video processing and high speed communications.

2:00 pm

Introduction

16.1

2:05 pm

Cochlear Implant Signal Processing ICs (INVITED PAPER), B. Swanson, M. Goorevich, T. Nygard, Cochlear Ltd., E. Van Baelen, K. Van Herck, Cochlear Technology Center, and M. Janssens, NXP

The Nucleus Freedom cochlear implant system enables a profoundly deaf person to hear. The system consists of a surgically implanted stimulator and a battery-powered external sound processor. The processor is based on a 0.18 μm CMOS ASIC containing four DSP cores. The signal processing includes a two-microphone adaptive beamformer, a 22-channel quadrature FFT filterbank, multi-band automatic gain control, a psycho-acoustic masking model and non-linear compression. The key design challenge was power consumption.

16.2

2:55 pm

An 81.6 GOPS Object Recognition Processor Based on NoC and Visual Image Processing Memory, D. Kim, K. Kim, J.-Y. Kim, S. Lee and H.-J. Yoo, KAIST

An 81.6 GOPS object recognition processor is developed by using NoC and Visual Image Processing (VIP) memory. SIFT (Scale Invariant Feature Transform) objects recognition requires huge computing power and data transactions among tasks. The chip integrates 10 SIMD PEs for data/task level parallelism while the NoC facilitates inter-PE communications. The VIP memory searches local maximum pixel inside a 3x3 window in a single cycle providing 65.6 GOPS. The proposed processor achieves 15.9fps SIFT feature extraction at 200 MHz.

16.3

3:20 pm

A Cost-effective Digital Front-End Realization For 20-bit Sigma-Delta DAC in 0.13 μm CMOS, R. Chen, L. Liu and D. Li, Tsinghua University

A cost-effective digital front-end used in 20-bit sigma-delta DAC is described in this paper. It includes an interpolator and a sigma-delta modulator. Mixed-radix number representation algorithm combined with poly-phase filtering technique and high efficiency hardware realization method are used to achieve high data conversion precision and reduce the area of the interpolator. A single bit distributed feedback structure is adopted for DSM to shape quantization noise. The overall digital front-end achieves above 130dB dynamic range.

3:45 pm – Break

16.4

4:00 pm

A 0.25 μm 0.92mW per Mb/s Viterbi Decoder Featuring Resonant Clocking for Ultra-Low-Power 54Mb/s WLAN Communication, F. Carbognani, S. Haene, M. Arrigo, C. Pagnamenta, F. Buergin, N. Felber, H. Kaeslin and W. Fichtner, ETH Zurich

Resonant clocking is applied to a Viterbi decoder for ultra-low-power WLAN communication. Clock skew balancing and excessive cross-over currents are identified as the most relevant issues: H-clock-trees and a new latch circuit are proposed as power-efficient design solutions. The 30000 gate-equivalent core in a 0.25 μm CMOS process dissipates 50 mW at 54Mb/s throughput (1.75 V), with about 27% power savings compared to an equivalent circuit with one-phase single-edge-triggered clocking and a recently published competitor.

16.5

4:25 pm

A High-Throughput Maximum a posteriori Probability Detector, R. Ratnayake, G.-Y. Wei, Harvard University, A. Kavcic, University of Hawaii

This paper presents a maximum a posteriori probability (MAP) detector, based on a forward-only algorithm that can achieve high throughputs. The MAP algorithm is optimal in terms of bit error rate. The proposed detector utilizes a deep-pipelined architecture implemented in skew-tolerant domino and experimentally measured results verify the detector can achieve throughputs greater than 750MHz while consuming 2.4W. The detector is implemented in a 0.13 μ m CMOS technology and has a die area of 9.9 mm².

16.6

4:50 pm

A 3.3-Gbps Bit-Serial Block-Interlaced Min-Sum LDPC Decoder in 0.13 μ m CMOS, A. Darabiha, A. Chan Carusone and F. Kschischang, University of Toronto

A bit-serial architecture for multi-Gbps LDPC decoding is demonstrated to alleviate the routing congestion which is the main limitation for LDPC decoders. We report on a 3.3-Gbps 0.13- μ m CMOS prototype. It occupies 7.3-mm² core area with 1416-mW maximum power consumption from a 1.2-V supply. We demonstrate how early termination and supply voltage scaling can improve the decoder energy efficiency. Finally, the same architecture is applied to a (2048, 1723) LDPC code compliant with the 10GBase-T standard.

Session 17 – Wideband Techniques

Fir Ballroom, Tuesday Afternoon, September 18

Chair: Tony Chan Carusone

Co-Chair: Ed Van Tuijl

This session focuses on the design of high-speed wireline circuits for data connectivity up to 100 Gb/s. Novel architectures and methodologies are presented.

2:00 pm

Introduction

17.1

2:05 pm

A Heterodyne Phase Locked Loop with GHz Acquisition Range for Coherent Locking of Semiconductor Lasers in 0.13 μ m CMOS, F. Aflatouni, O. Momeni and H. Hashemi, USC

A heterodyne electro-optical phase-locked loop (EOPLL) architecture is proposed that can lock the frequency and phase of semiconductor lasers. An aided-acquisition circuit inspired by the combination of RF image-rejection receivers and digital PLL architectures is used to extend the frequency-acquisition range. An integrated circuit prototype is implemented in a 0.13 μ m CMOS technology and includes a wideband transimpedance amplifier and PLL circuitry. Measurement results for the locking of Vertical Cavity Surface Emitting Lasers are reported.

17.2

2:30 pm

A Synthesis-based Bandwidth Enhancing Technique for CML Buffers/Amplifiers, D. Pi, B.-K. Chun and P. Heydari, University of California

A synthesis-based bandwidth enhancing technique for current-mode-logic (CML) buffers/amplifiers is presented, which achieves bandwidth-enhancement-ratio (BWER) of 4.84, close to a proven theoretical upper limit of 4.93. By employing a complete step-by-step design methodology, the proposed technique can be applied to any load condition, which is characterized by the ratio between the load capacitance and the output capacitance of the transconductor cell. Several prototype buffer/amplifier circuits are designed using lower order passive networks to save chip area. The test chip is fabricated in a 0.18 μm CMOS process, and measurements show a BWER of 3.8.

17.3

2:55 pm

Towards a sub-2.5V, 100-Gb/s Serial Transceiver (INVITED PAPER), S. Voinigescu, R. Aroca, S. Nicolson, T. Chalvatzis, University of Toronto, P. Chevalier, P. Garcia, C. Garnier and B. Sautreuil, STMicroelectronics, T. Dickson, IBM

This paper describes first a half-rate, 2.5V, 1.4W, 87-Gb/s transmitter with on-chip PLL fabricated in a production 130nm SiGe BiCMOS process. Next, the most critical blocks required for the implementation of a full-rate 100-Gb/s serial transceiver are explored. State-of-the art 105-GHz, SiGe HBT static frequency dividers and VCOs operating from 2.5V, as well as 65-nm CMOS, 1.2V, 90-GHz static frequency dividers, low-phase noise VCOs, and 100-GHz clock distribution network amplifiers are fully characterized.

3:45 pm - Break

17.4

4:00 pm

Future Microprocessor Interfaces: Analysis, Design and Optimization (INVITED PAPER), B. Casper, G. Balamurugan, J. Jaussi, J. Kennedy, M. Mansuri, F. O'Mahony and R. Mooney, Intel Corporation

High-aggregate bandwidth interfaces with minimized power, silicon area, cost and complexity will be essential to the viability of future microprocessor systems. Optimization of microprocessor interfaces at the system level is crucial to providing the most cost-effective and efficient solution. This paper details a comprehensive interconnect and system level analysis method that can be used to accurately evaluate platform-level tradeoffs and has been correlated to link measurements with 10% accuracy. System tradeoffs with respect to interconnect quality, equalization, modulation, clock architecture are shown. Interconnect and circuit density improvements are identified as a promising research direction to maximize the bandwidth and power efficiency of future microprocessor platforms.

17.5

4:50 pm

Time-Variant Characterization and Compensation of Wideband Circuits, A. Amirkhany, M. Horowitz, Stanford University, A. Abbasfar, J. Savoj, Rambus, Inc.

Many wideband circuits use interleaving to extend bandwidth leaving them with a cyclically time-variant output. This paper describes a technique for characterization of these types of circuits based on Least-Squares Estimation of the time-varying response of circuits. Applying the methodology to a 90-nm, 12-GS/s 8-bit digitally-equalized DAC, shows significant timing varying behavior. Furthermore, using the data obtained from characterization to construct linear time-variant compensation improves the DAC signal-to-distortion ratio by at least 6 dB.

17.6

5:15 pm

High-Voltage-Tolerant I/O Circuit Design for USB 2.0-Compliant Applications, M.-J. Kim, T.H. Lee, Stanford University, H. Icking, H. Gossner, Infineon Technology

We present design strategies of high-voltage tolerant I/O circuits for interfaces of 3.3V or higher. The test vehicle is a USB 2.0-compliant I/O circuit. This is a challenging example because USB 2.0 requires substantial over-voltage tolerance from -1V to 5.25V. In addition, USB 2.0 requires continuous monitoring of this condition and protection when no power is present. The proposed concept is demonstrated in a 90nm CMOS process.

Session 18 – Compact Modeling for Analog and RF

Pine Ballroom, Tuesday Afternoon, September 18

Chair: Rob Jones

Co-Chair: Hong-Ha Vuong

This session presents advanced compact models and modeling/synthesis approaches to address analog and RF applications.

2:00 pm

Introduction

18.1

2:05 pm

PSP-Based Scalable MOS Varactor Model, (INVITED PAPER), J. Victory, Z. Yan, J. Cordovez, Jazz Semiconductor, Z. Zhu, Q. Zhou, W. Wu, G. Gildenblat, Arizona State University, C. McAndrew, Freescale Semiconductor, F. Anderson, IBM, J. Paasschens, NXP Semiconductors, R. van Langevelde, Philips Research, P. Kolev, Qualcomm, R. Cherne, Intersil Corp. and C. Yao, Analog Devices

18.2

2:55 pm

An Accurate Scalable Compact Model for the Substrate Resistance of RF MOSFETs, B. Parvais, M. Dehan, A. Mercha, S. Decoutere, IMEC, S. Hu, Shanghai IC R&D Center

A new scalable compact model for the substrate resistance of multi-finger MOSFETs is presented and validated up to 50 GHz on a 90 nm CMOS technology. The physical foundation, used to capture the 2D distributed nature of the well resistance, provides a more accurate description of different layout styles over a wide range of geometries. The model is used to determine the folding for minimum substrate resistance and is implemented straightforwardly with the PSP model.

18.3

3:20 pm

Synthesis of Optimal On-Chip Baluns, S. Kapur, D. Long, R. Frye, Integrand Software, Y.-C. Chen, M.-H. Cho, H.-W. Chang, J.-H. Ou and B. Hung, UMC

We describe a method for synthesizing on-chip baluns. The method involves creating a scalable transformer model from electromagnetic simulations, followed by a search through design space to find an optimal balun. We used this method to design 90nm RFCMOS baluns. The baluns have insertion loss less than 1.5dB, phase imbalance of 0.25 degrees and amplitude imbalance of 0.25dB. These characteristics are equal to or better than off-chip baluns while requiring significantly less area.

3:45 pm – Break

18.4

4:00 pm

An Integrated Modeling Paradigm of Circuit Reliability for 65nm CMOS Technology, W. Wang, R. Vattikonda, Y. Cao, Arizona State University and V. Reddy, A. Krishnan, S. Krishnan, Texas Instruments

The de facto modeling method to analyze channel-hot-carrier (CHC) is based on substrate current (I_{sub}), which becomes increasingly problematic with technology scaling as various leakage components dominate I_{sub} . In this work, we present a unified approach that directly predicts the change of key transistor parameters under various process and design conditions, for both negative-bias-temperature-instability (NBTI) and CHC degradation. Using the general reaction-diffusion model and the concept of surface potential, the proposed method continuously captures the performance degradation across subthreshold and strong inversion regions. Models are comprehensively verified with an industrial 65nm technology. We benchmark the prediction of circuit performance degradation with measured ring oscillator data and simulations of an amplifier.

18.5

4:25 pm

Mismatch Characterization of Ring Oscillators, A. Balankutty, T.-C. Chih, C.-Y. Chen and P. Kinget, Columbia University

We investigate frequency matching of ring oscillators to study matching of non-static operation of identical high speed analog, digital and RF circuits. The oscillator test structures on a 0.25 μm CMOS technology operate in the 500MHz to 3GHz range. The non-static matching experimental results are compared to predictions based on DC matching parameters. Stage averaging versus device size averaging for constant frequency designs is investigated. Global variations and long distance matching are also examined and compared.

18.6

4:50 pm

The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design (INVITED PAPER), C. Galup-Montoro, M. Schneider, O. Siebel, Federal University of Santa Catarina, A. Cunha, Federal University of Bahia, F. Sousa, Federal University of Rio Grande do Norte, and H. Klimach, Federal University of Rio Grande do Sul

Most of the new generation compact models for the MOSFET have many commonalities since they are based on the same main approximations: gradual channel, charge-sheet, and depletion charge linearization. In this study we show that if we include some additional physics-consistent conditions for the MOSFET equations we obtain a very compact model that we call the advanced compact MOSFET (ACM) model. The core ACM model, design-oriented equations, parameter extraction, and a design example are presented.

Session 19 – Front-Ends and Synthesizers for Communication Applications

Cedar Ballroom, Tuesday Afternoon, September 18

Chair: Ranjit Gharpurey

Co-Chair: Rick Carley

This session begins with presentations on four receiver front ends, covers two frequency synthesizers, and finishes with a high efficiency CMOS cellular power amplifier.

2:00 pm

Introduction

19.1

2:05 pm

A 3.5mW 900MHz Down-converter with Multiband Feedback and Device Transconductance Reuse, J. Han and R. Gharpurey, University of Texas Austin

A down-converter is presented wherein the IF-output of a mixer is applied to its input transistor to enhance gain without increasing bias current. A 900MHz receiver with power dissipation of 3.5mW is demonstrated in a 0.13 μm CMOS process. The conversion gain is variable from 10-50dB, the NF is 9.8dB at peak gain and the OIP3 is 8dBV-p. The receiver has a third-order low-pass response at IF. The area requirement is 0.1mm².

19.2

2:30 pm

A Highly Linear Broadband Variable Gain LNA for TV Applications, D. Manstretta, Università degli Studi di Pavia, and L. Dauphinee, Broadcom Corp.

A broadband variable-gain LNA with triple output for TV tuners has been demonstrated in a 0.18 μm SiGe technology. The gain varies continuously from 27dB to -28dB and has better than 1dB precision over a 1GHz bandwidth. At 27dB gain the amplifier shows 6.5dB NF, 82dBmV OIP3 and 121dBmV OIP2. OIP3 is above 73dBmV down to -21dB gain. With all three outputs enabled the circuit draws 170mA from a 3.3V supply.

19.3

2:55 pm

A Current-Equalized Distributed Receiver Front-End for UWB Direct Conversion Receivers, A. Safarian, L. Zhou and P. Heydari, University of California Irvine

A power-efficient distributed direct-conversion RF front-end (DDC-RF) circuit, using merged LNA/mixer cells, presented for UWB systems. A current-equalization technique was implemented to remove systematic IQ phase/gain mismatches. The DDC-RF prototype in 0.13 μm CMOS with the use of programmable input matching achieved average gain of 14.3dB and NF of 5.7dB over the UWB. The IQ gain/phase imbalances are less than $\pm 0.5\text{dB}/\pm 2.5\text{degree}$, respectively. The current consumption is 8mA from 1.8V.

19.4

3:20 pm

A 65 μW , 1.9 GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Nodes, N. Pletcher, S. Gambini and J. Rabaey, University of California, Berkeley

A complete 1.9GHz receiver, with BAW resonator-referenced input matching network, is designed as a wakeup receiver for wireless sensor networks. The 90nm CMOS chip includes RF amplifier, PGA, ADC, and reference generation, while consuming 65 μW from a single 0.5V supply. The input RF bandwidth of the receiver is 7MHz, while the maximum data rate is 100kbps. When detecting a 31-bit sequence, the receiver exhibits -56dBm sensitivity for 90% probability of detection.

3:45 pm – Break

19.5

4:00 pm

A 4GHz Low Complexity ADPLL-based Frequency Synthesizer in 90nm CMOS, J. Zhuang, Q. Du and T. Kwasniewski, Carleton University

A 4GHz ADPLL-based integer-N frequency synthesizer is reported in this paper. It employs a low-complexity digital phase and frequency detector as well as a non-linear phase and frequency decision circuit to significantly reduce the hardware complexity while maintain a comparable in-lock performance to other high-complexity ADPLLs. The ADPLL was fabricated in 90nm CMOS technology to prove its feasibility. Operating with an high-frequency-resolution DCO, the proposed low-complexity ADPLL exhibits a programmable loop bandwidth from 100kHz to 6MHz with and an excellent in-band phase noise performance.

19.6

4:25 pm

A 4.2 GHz PLL Frequency Synthesizer with an Adaptively Tuned Coarse Loop, T. Wu, Rambus Inc., P. Hanumolu, K. Mayaram and U.-K. Moon, Oregon State University

A 4.2 GHz integer-N PLL frequency synthesizer for WLANs is described. An analog split tuned LC-VCO is controlled by coarse and fine loops to achieve both a large frequency tuning range and a small VCO gain. An averaging varactor is employed to reduce the amplitude sensitivity of the varactor, thereby reducing the AM-to-FM noise conversion. A new adaptively tuned switched capacitor integrator is used in the coarse loop for a fast lock time. The prototype test chip in a 0.13- μm CMOS process has a measured phase noise of -110dBc/Hz at 1 MHz offset, and a settling time of 50 μs .

19.7

4:50 pm

A 1.7-GHz 31dBm differential CMOS Class-E Power Amplifier with 58% PAE, R. Brama, L. Larcher, A. Mazzanti, Universita di Modena e Reggio Emilia and F. Svelto, Universita di Pavia

This paper shows that CMOS Class-E PAs are capable of high efficiency, even when delivering large output powers at RF. A cascode device is used to assure reliable operation. A differential solution has been adopted to maximize 2nd harmonic suppression and minimize potential on-chip interference. Prototypes realized in 0.13 μm CMOS technology show 31dBm maximum output power at 1.7GHz with 67% drain efficiency and 58% PAE, -51dBc and -39.5dBc suppression for 2nd and 3rd harmonics, respectively.

Poster Session

Cascade Ballroom, Tuesday Afternoon, September 18

5:30 pm – 7:30 pm

(Authors are at the posters from 5:30 pm – 7:00 pm)

TP-01

A 2.4GHz Efficiency-Enhanced Rectifier for Wireless Telemetry, K.-H. Chen, J.-H. Lu and S.-I. Liu, National Taiwan University

A 2.4GHz full-wave rectifier for wireless telemetry applications is presented. A conventional full-wave rectifier using diode-connected MOS transistors suffers from the power loss due to the intrinsic threshold voltage. In this paper, a full-wave rectifier using a transformer is presented. It has been fabricated in a 0.18 μm CMOS process. When input power ranges from 6dBm~12dBm, this proposed rectifier improves the efficiency of 2.5% compared with the conventional one.

TP-02

Comparative Studies of Common Control Schemes for Reference Tracking and Application of End-point Prediction, Y. Wu and P. K. T. Mok, Hong Kong University of Science and Technology

This paper analyzes the reference tracking behavior of Buck converters using several control schemes including voltage-mode, current-mode and V2-control from both large-signal and small-signal domains. Loop gains applicable to reference tracking are highlighted, and reference-to-output transfer functions are derived for the cases when end-point prediction (EPP) is applied to enhance the response. A novel V2-controlled Buck converter with EPP is fabricated. The measured reference tracking response shows 10 times improvement in speed.

TP-03

An Energy Management Circuit for Self-Powered Ubiquitous Sensor Modules, J. Pan and Y. Inoue, Waseda University

An energy management circuit is proposed for self-powered ubiquitous sensor modules using vibration-based energy. With the proposed circuit, the sensor modules work with low duty cycle operation. Moreover, a two-tank circuit as a part of the energy management circuit is utilized to solve the problem that the average power density of ambient energy always varies with time while the power consumption of the sensor modules is constant and larger than it. In addition, the long start-up time problem is also avoided with the timing control of the proposed energy management circuit. The CMOS implementation and silicon verification results of the proposed circuit are also presented. Its validity is further confirmed with a vibration-based energy generation. The sensor module is used to supervise the vibration of machines and transfer the vibration signal discontinuously. A piezoelectric element acts as the vibration-to-electricity converter to realize battery-free operation.

TP-04

An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes, M. Seeman, S. Sanders and J. Rabaey, University of California Berkeley

A power interface IC is designed and demonstrated to convert and manage power for a wireless tire pressure sensor node. Power conversion is performed using on-chip switched-capacitor converters with size-optimized devices and level-shifting gate drivers. A synchronous rectifier efficiently harvests energy from an electromagnetic shaker and control circuitry regulates the output voltage while minimizing power consumption. The converters achieve efficiencies approaching 80%.

TP-05

A Low Standby Power Flip-flop with Reduced Circuit and Control Complexity, L. Clark, M. Kabir and J. Knudsen, Arizona State University

A flip-flop using thin and thick gate transistors combines high performance and low standby power. The design has reduced circuit and power-down control complexity compared to previous circuits using thick gate shadow latches for low standby power state storage. Measured test chip results on a foundry 130 nm process prove the viability of the design. Reduced shadow latch supply voltage during standby is shown to be effective at mitigating the drain to bulk leakage components.

TP-06

A 610-MHz FIR Filter Using Rotary Clock Technique, Z. Yu and X. Liu, North Carolina State University

This paper presents a novel FIR filter design based on a resonant clocking technique called rotary clock. It utilizes the spatially distributed multiple rotary clock phases and achieves the full rotary clock power saving potential. Our filter operates at 610 MHz, delivering a throughput of 39 Gbps. In comparison with the conventional clock tree based design, it achieves a 34.6% clocking power saving and a 12.8% overall circuit power reduction.

TP-07

A 186Mvertices/s 161mW Floating-Point Vertex Processor for Mobile Graphics Systems, C.-H. Yu, K. Chung, D. Kim and L.-S. Kim, KAIST

In this paper, a power-efficient vertex processor with a geometry-specific arithmetic unit, vertex caches, and a vertex texturing unit is presented for mobile graphics environments. The proposed vertex processor achieves 186 Mvertices/s of geometry performance which is 1.6 times faster than the previous results among the IEEE754-compliant arithmetic units, and it supports OpenGL ES 2.0 and Vertex Shader Model 3.0. The processor is implemented in a 0.18- μm 1P4M CMOS process.

TP-08

A 0.8-1.2GHz Single-Phase Resonant-Clocked FIR Filter with Level-Sensitive Latches, V. Sathe, J. Kao and M. Papaefthymiou, University of Michigan

In this paper we present the design and experimental validation of RF1, a 0.8-1.2GHz frequency-scalable, resonant-clocked FIR filter test-chip with level-sensitive latches. Designed using a fully automated ASIC flow, RF1 was fabricated in a 130nm CMOS process with an on-chip inductor and clock generator. At its resonant frequency of 1.03GHz, RF1 dissipates 132mW, with clock power accounting for 10.8% of total power dissipation. Resonating 42pF of clock load, RF1 achieves 76% clock-power efficiency over CV^2f .

TP-09

Addressing Parametric Impact of Systematic Pattern Variations in Digital IC Design, P.-H. Wang, B. Lee, G. Han, UMC, R. Rouse, P. Hurat and N. Verghese, Clear Shape Technologies

A simulation methodology to predict changes in circuit characteristics due to systematic lithography and etch effects is described. This methodology is used to update an existing circuit netlist to produce accurate delay calculation and is silicon validated using various transistor and ring oscillator structures. In a digital IC design flow, the delay variation due to lithography and etch is calculated and used to identify and repair timing "hotspots" or parametric failures due to systematic variations.

TP-10

Design Considerations and Benefits of Three-Dimensional Ternary Content Addressable Memory, E. C. Oh and P. Franzon, North Carolina State University

Three dimensional (3D) ternary content addressable memory (TCAM) has been designed in a 0.18 μm fully depleted silicon on insulator (FD SOI) 3D IC process. This paper demonstrates that a 3D TCAM with three tiers can achieve 40% matchline capacitance reduction and 21% power reduction compared to a TCAM in a conventional single-tier process. This paper also discusses design considerations of 3D TCAM including partitioning methods for multiple tiers and layout methods of interconnects.

TP-11

A 37 ppm/ $^{\circ}\text{C}$ Temperature Compensated CMOS ASIC with $\pm 16\text{ V}$ Supply Protection for Capacitive Microaccelerometers, H. Ko, S.-J. Paik, B. Choi, D.-I. Cho, Seoul National University, and A. Lee, T. Ahn, SML Electronics

A high reliability CMOS-MEMS hybrid microaccelerometer system is presented. To enhance the temperature response and to minimize die-to-die variations, a low-noise continuous-time front-end architecture with temperature-compensation and parasitic-cancellation is proposed. The temperature coefficients of the output bias and the scale factor are measured to be 37 ppm/ $^{\circ}\text{C}$ and 27 ppm/ $^{\circ}\text{C}$, respectively. The bias instability level is measured to be 42 μg . The integrated $\pm 16\text{ V}$ supply protection gives the enhanced system reliability and reduced form-factor.

TP-12

A 500 MHz Low Phase-Noise A1N-on-Silicon Reference Oscillator, H. M. Lavasani, R. Abdolvand and F. Ayazi, Georgia Institute of Technology

This paper presents a 496MHz reference oscillator using a high-Q lateral-mode AIN-on-Si micromechanical resonator that does not require DC voltage for operation. The sustaining amplifier consists of an inductorless high-gain CMOS transimpedance amplifier that is optimized for low phase-noise. The resonator is designed to have high quality factor in air ($Q \sim 3800$) with low impedance. The measured phase-noise at 1kHz is -92dBc/Hz with phase-noise floor below -147dBc/Hz (exceeding GSM phase-noise requirement by 2dB and 28dB, respectively).

TP-13

1.1 TMACS/mW Load-Balanced Resonant Charge-Recycling Array Processor, R. Karakiewicz, R. Genov, University of Toronto and G. Cauwenberghs, University of California San Diego

A resonant adiabatic mixed-signal 128x256 array processor achieves 1.1 TMACS (tera-multiply-accumulates per second) per mW of power from a 1.6V DC supply. The 1.9x9 sq. micron 3T NMOS unit cell with single-wire pitch multiplexed bit/compute line provides charge-conserving 1b-1b multiplication

and single-wire analog accumulation. A stochastic data modulation scheme minimizes on-chip capacitance variability maintaining clock oscillations near resonance.

TP-14

Optimization of SC Sigma Delta Modulators based on Worst-Case-Aware Pareto-Optimal Fronts,
J. Zou, H. Graeb, D. Mueller and U. Schlichtmann, Techn. Univ. Muenchen

This paper presents an optimization method for switched-capacitor sigma-delta modulators. The SNR performance is maximized while considering the performance capability of the critical building block, i.e. the Op Amp. Performance space exploration is applied to find the feasible region of the building block's performance, which is represented by a Pareto optimal front. Through worst-case analysis on design points of the nominal Pareto front, a worst-case-aware Pareto-optimal front can be computed. The maximized SNR and the corresponding yield will be presented. The proposed optimization process is efficient and can be accomplished in some hours.

TP-15

Obtaining Frequency Sensitivities to Variations Analytically from Parameterized Nonlinear Oscillator Phase Macromodels,
Z. Wang and J. Roychowdhury, University of Minnesota

System-level variability analysis and design centering for oscillators relies on fast and accurate methods for obtaining the parametric sensitivities of higher-level performances (such as center frequency) directly from phase macromodels. We present an efficient and elegant method, involving no numerical simulation, for finding parametric sensitivities of oscillator frequencies directly from nonlinear phase domain macromodels. We validate the method, termed FS-PPV, on numerically extracted ring and LC oscillator PPV macromodels, as well as on a purely analytical exact PPV macromodel for idealized ring oscillators. We apply FS-PPV to find statistical distributions of oscillator center frequencies and validate these distributions against Monte-Carlo simulations. FS-PPV achieves speedups of more than 3000x.

TP-16

Modeling and Validation of Silicon Contour-Based Extraction and Simulation of Non-Uniform Devices,
T. Devoivre, STMicroelectronics, R. Rouse, N. Verghese and P. Hurat, Clear Shape Technologies

A current density-based model is proposed to predict the drawn current of transistors that exhibit non-uniform geometry. Using the active and poly contours of the actual transistor shape from a lithography-like simulation, the current density model is integrated over the transistor width to obtain its drawn current and equivalent transistor parameters for circuit simulation. Comparison to Silicon drive current measurements of Poly T and Active T structures on a ST 65nm process show excellent correlation.

TP-17

Standard Cell and Custom Circuit Optimization using Dummy Diffusions through STI Width Stress Effect Utilization,
R. O. Topaloglu, University of California

Starting at the 65nm node, stress engineering to improve performance of transistors has been a major industry focus. An intrinsic stress source - shallow trench isolation - has not been fully utilized up to now for circuit performance improvement. In this paper, we present a new methodology that enables the exploitation of STI stress for performance improvement of standard cells and custom integrated circuits. We start with process simulation of a 65nm STI technology, and generate mobility models for STI stress based on these simulations. Based on these models, we are able to perform STI stress-aware modeling and simulation using SPICE. We then present our optimization of STI stress in standard-cell and custom designs using active-layer (dummy) fill insertion to alter the STI widths. Circuit level experimental results are based on a miscellaneous ring oscillator, which is known to correlate well to silicon. Using a generic 65nm cell library, we show that the STI-optimized designs provide up to 8% improvement in clock frequency. The frequency improvement through exploitation of STI stress comes at practically zero cost with respect to area and wirelength.

TP-18

FinFET SRAM: Optimizing Silicon Fin Thickness and Fin Ratio to Improve Stability at iso Area, D. Lekshmanan, A. Bansal and K. Roy, Purdue University

In FinFET SRAM, width quantization and variation in silicon thickness are major challenges impacting stability and manufacturability. We propose a methodology to improve the stability of an SRAM cell by co-optimizing the different transistor fin combinations (sizing of different transistors) and silicon thickness (of FinFET) at iso-area. At iso-area, read SNM can be increased approx. 2X by varying fin-combination while decreasing write margin by 17%. Further, at iso-area and stability, we propose that silicon fin thickness constraint can be relaxed in FinFETs to improve the manufacturability and reduce process variability. Increasing the silicon fin thickness by approx. 50%, degrades read SNM by 10% while negligibly affecting write margin and increasing access time by 36%. Increased silicon thickness reduces body thickness variation in FinFETs, resulting in reduced device mismatch among transistors in an SRAM cell.

TP-19

A Comprehensive Phase-Transfer Model for Delay-Locked Loops, J. Burnham, Stanford University, G.Y. Wei, Harvard University, C.-K. K. Yang, UCLA, and H. Hindi, PARC

This paper presents a comprehensive model for analyzing the behavior of an analog delay-locked loop (DLL). Unlike previous models, the proposed version includes both constant and variable phase-offset terms, making it possible to calculate jitter transfer characteristics, stability, and static phase errors from a single unified model. The topology more closely approximates the underlying architecture of the DLL, resulting in improved accuracy and enabling better tradeoffs between bandwidth, stability, and power.

TP-20

Efficient Frequency-Domain Simulation of Massive Clock Meshes Using Parallel Harmonic Balance, W. Dong, P. Li and X. Ye, Texas A&M University

High performance IC designs impose stringent design specifications on clock distribution networks, where clock skews must be well controlled even under the presence of environmental and process variations. As a result, clock meshes are gaining increasing popularity due to their inherent low skew and immunity to variations. While clock meshes are often analyzed in time-domain for the purpose of verification as well as tuning, the massive couplings within the passive mesh structure and in between a large number of clock drivers are challenging to handle. In contrast, frequency-domain steady-state simulation techniques such as harmonic balance (HB) are specifically advantageous since the massive passive mesh structure can be rather compactly represented using matrix transfer function matrices at a discrete set of harmonic frequencies. The remaining challenge, however, is to develop harmonic balance techniques that can efficiently simulate highly nonlinear steady-state problems corresponding to a large number of tightly coupled clock drivers. In this paper, we present a hierarchically preconditioned algorithm that is particularly suitable to clock mesh analysis. Moreover, we show that the parallelizable nature of our algorithm allows further runtime improvement of large clock mesh analysis via parallel processing.

TP-21

Low-Voltage Multi-Mode G_m -C Channel Selection Filter for Mobile Applications, T.-Y. Lo and C.-C. Hung, National Chiao Tung University

A third-order Butterworth low-pass filter implemented with the transconductors was designed by TSMC 0.18- μm CMOS process. The measurement results show that the tuning range and the linearity performance would be suitable for the wireless specifications of GSM, Bluetooth cdma2000, and Wideband CDMA. In the design, the maximum power consumption at the highest cutoff frequency is 2 mW under a 1-V supply voltage.

TP-22

Multi-Mode Modulator and Frequency Demodulator Circuits for Gb/s Data Rate 60 GHz Wireless Transceivers, A. Valdes-Garcia, S. Reynolds and T. Beukema, IBM TJ Watson

Compact RF circuits that enable Gb/s wireless links on integrated 60 GHz radios are presented. A multi-mode modulator performs a variety of signaling schemes including MSK directly from a digital bit-stream and also performs the IF up-conversion. An FM discriminator operates at an IF frequency of 9 GHz with a sensitivity of -70 dBm referred to the RF input and yields an output digital bit stream. Implemented in a SiGe 0.13 μm BiCMOS process as part of a transceiver chipset, the modulator and demodulator occupy an area of only 0.03mm² and 0.02mm², respectively. The performance of the proposed circuits is verified individually and also in a HDTV 2 Gb/s MSK link.

TP-23

CMOS Low Noise Amplifier with Capacitive Feedback Matching, E. Adabi and A. Niknejad, University of California Berkeley

A capacitive shunt feedback LNA input matching network is demonstrated which offers matching, good noise performance, low component count and low area consumption. A prototype 9GHz LNA vehicle amplifier is designed and fabricated in a 130nm RF-CMOS process. The measured amplifier has 20.5dB of gain at 8.8GHz with input and output match of -15dB and -8dB respectively. It has 1.4GHz of 3dB-bandwidth around 9GHz with the noise figure of 1.7dB at the center frequency and below 2dB across the band. Large signal measurements reveal that the amplifier can deliver -2dBm of power to the 50 ohm output load at its 1dB compression point. It draws 23mA of current from a 1.2V supply. The chip occupies an area of 0.64mm².

TP-24

A 750Mb/s 12pJ/b 6-to-10GHz Digital UWB Transmitter, V. Kulkarni, M. Muqsith, H. Ishikuro and T. Kuroda, Keio University

In this paper, an all-digital, ultra-wideband transmitter in 0.18 μm CMOS is presented. The transmitter realizes Bi-phase modulation scheme and generate 500ps duration pulses with center frequency of 8GHz. Measured results show that the transmitter consumes 12pJ/b to achieve data rate of 750Mb/s. An optional embedded on-chip antenna and a power amplifier operating in 6-10GHz band are also designed as a future low cost solution for short distance communications.

TP-25

A 3.1-8.0 GHz MB-OFDM UWB Transceiver in 0.18 μm CMOS, H. Zheng, S. Lou, D. Lu, C. Shen, T. Chan and H. Luong, The Hong Kong University of Science and Technology

This paper presents a complete CMOS dual-conversion zero-IF² transceiver for 9-band MB-OFDM UWB systems from 3.1 to 8.0 GHz. The transceiver integrates all building blocks including a variable-gain wideband LNA, a single mixer for both RF down and up conversions in RX and TX, a fast-settling frequency synthesizer, and IQ ADCs and DACs. Fabricated in a standard 0.18- μm CMOS process, the receiver measures maximum S11 of -13dB, maximum NF of 8.25 dB, in-band IIP3 of better than -13.7 dBm, and variable gain from 25.3 to 84.0 dB. IQ path gain and phase mismatch of the receiver chain are measured to be 0.8 dB and 4 \circ respectively. The transmitter achieves a minimum output P-1dB of -8.2 dBm, sideband rejection of better than -42.2 dBc, and LO leakage of smaller than -46.5 dBc.

TP-26

A -90dBm Sensitivity 0.13 μm CMOS Bluetooth Transceiver Operating in Wide Temperature Range, K. Agawa, H. Majima, H. Kobayashi, M. Koizumi, S. Ishizuka, T. Nagano, M. Arai, Y. Shimizu, G. Urakawa, N. Itoh, M. Hamada and N. Otsuka, Toshiba Corporation

A 2.4GHz 0.13 μm CMOS transceiver achieves high performance between -40C and +90C. A low-IF receiver and direct-conversion transmitter architecture is employed. A temperature compensated receiver chain including LNA achieves a high sensitivity of -89.6dBm even in the worst environmental condition. Linearity optimization for a transmitter chain including a variable biasing circuit in PA reduces the second harmonics of TX signals so that it suppresses the VCO pulling and keeps the carrier frequency drift within 18kHz.

TP-27

On IIP2 Improvement by Injecting DC Offset at the Mixer in a Wireless Receiver, I. Elahi and K. Muhammad, Texas Instruments

We present a digital calibration technique for improving IIP2 by injecting DC offset at the mixer. By controlling amplitude of the injected DC, IIP2 degradation due to LO leakage at the input of RF amplifiers can be compensated. Mathematical analysis and measurement data for a quad-band GSM/GPRS receiver implemented in 90-nm digital CMOS process are presented. Calibrated IIP2 of 50dBm is reported at LNA input.

TP-28

ECO chip: Energy Consumption Zeroize Chip with a 953MHz High-Sensitivity Radio Wave Detector for Standby Mode Applications, T. Umeda and S. Otaka, Toshiba R&D Center

ECO chip (energy consumption zeroize chip) for standby mode applications is presented. ECO chip detects 953MHz band radio waves from a remote control (RC) by using a high-sensitivity rectifier and switches on/off the main power supplies of applications with ultra-low power consumption. Sensitivity of -42dBm and communication distance of 10m from 13dBm output RC are achieved with 0.14uW power consumption.

TP-29

On the Transient Behavior of Injection Locked LC Oscillators, N. Lanka, S. Patnaik and R. Harjani, University of Minnesota

An analytical framework has been developed to describe the transient behavior of negative resistance injection-locked oscillators based on Adler's equation. Design insights are provided by using a combination of analytical simplifications and graphical interpretation. It has been shown that injection locking can be used to meet the requirements for fast hopping systems like the MBOA-UWB specification. The theoretical analysis and design solutions have been verified by extensive simulations on real CMOS processes.

TP-30

A Wideband CMOS Linear Digital Phase Rotator, H. Wang and A. Hajimiri, California Institute of Technology

This paper presents a 10-bit wideband Cartesian phase rotator with a novel linear digital VGA implemented in a 0.13 μm CMOS process. The VGA topology is robust to device modeling uncertainties and PVT variations. The system provides 7.8dB voltage gain with -3dB bandwidth of 7.6GHz. A maximum phase error of 2° has been achieved for a phase shifting range of 360° with 32 phase steps of 11.25°. The capability to compensate for mismatched quadrature inputs is also demonstrated.

TP-31

Low-Power CMOS Energy Detection Transceiver for UWB Impulse Radio System, T.-A. Phan, V. Krizhanovskii, S.G. Lee, Information and Communications University

This paper presents an ultra low-power non-coherent transceiver (TRx) operating in 3-5 GHz band using energy detection (ED) receiver for impulse radio ultra-wideband (IR-UWB) systems. The proposed low-complexity ED receiver consists of a wideband LNA, a squarer, an analog integrator, and a sample and hold circuit, of which only the LNA consumes static current. The transmitter consists of a pulser which is based on the ON/OFF operation of an LC oscillator. Fabricated in 0.18- μm CMOS technology with 1.5 V supply, measurements show the FCC-compliant output pulses with the duration of 3.5 ns, which corresponds to 520 MHz bandwidth. Maximum pulse rate is up to over 200 MHz. The pulser dissipates only the dynamic current with average energy of 16.8 pJ per pulse, and the receiver dissipates 3.5 mA of static current. The receiver shows 9 dB of NF and a sensitivity of -70 dB. Transceiver die size is 1.3 x 1mm.

Session 20 – Analog Techniques

Oak Ballroom, Wednesday Morning, September 19

Chair: Don Thelen

Co-Chair : Dennis Fischette

This session presents analog circuit design techniques used in frequency selective filters, image sensors, and temperature and process compensated oscillators.

8:25 am

Introduction

20.1

8:30 am

An 80MHz Noise Optimized Continuous-Time Bandpass Filter in 0.25 μ m BiCMOS, A. Kumar and P. Allen, Georgia Institute of Technology

An 80 MHz bandpass filter with a tunable quality factor of 16~44 using an improved transconductor circuit is presented. The noise optimized biquad structure achieves SNR of 45dB at IMD of 40dB. The P-1dB compression point and IIP3 of the filter are -10dBm and -2.68dBm, respectively. The proposed filter gives an output of 1.87Vpp at -1dB compression point in 3.3V supply and consumes 66mW. It is fabricated in 0.25 μ m BiCMOS.

20.2

8:55 am

A Low Power 44-300 MHz Programmable Active-RC Filter in 0.18 μ m CMOS, T. Laxminidhi, V. Prasadu and S. Pavan, Indian Institute of Technology-Madras

We present a widely programmable fifth order Chebyshev opamp-RC ladder filter whose 3 dB bandwidth is digitally tunable over a 7X range, from 44-300 MHz. The opamp uses feed-forward compensation to achieve high DC gain and wide bandwidth with reduced bias currents. The principle of "constant capacitance scaling" is used to maintain the shape of the filter response when the bandwidth is changed by a large factor. The filter consumes 36 mW from a 1.8V supply and has a dynamic range of 56.6 dB.

20.3

9:20 am

A Q-enhanced Transformer Coupling Dynamic Dual-Mode 5GHz Bandpass NB / Interference Rejection UWB Filter, B. Pham and A. Dinh, University of Saskatchewan

This paper presents a fully integrated dual mode Q-enhanced bandpass/notch filter front-end designed for Narrowband and UWB receivers. Using a simple logic state to switch its function, the filter can provide bandpass filtering for channel selection in the NB mode or NB interference rejection in the UWB mode. A Q-enhanced circuit coupled through a transformer is used to realize the modes. Using 1.8V supply, the filter consumes 22 mW of power and provides a 32dB interference rejection in the UWB mode and a gain of 24dB in the NB mode. The design occupies a die area of 1mm² using the mainstream 0.18 μ m CMOS process.

20.4

9:45 am

A Process and Temperature Compensated Two-Stage Ring Oscillator, K. Lakshmikummar, V. Mukundagiri and S. Gierkink, Conexant Systems

Local positive feedback in a delay element enables a ring oscillator with only two stages to oscillate and produce quadrature clocks. Routh-Hurwitz's criterion is applied to prove that such a structure can

oscillate. An internally generated power supply from a constant-gm bias keeps the free running frequency to within $\pm 5\%$ from -40 to 125°C over process variations. The 1.25GHz oscillator in $0.13\ \mu\text{m}$ CMOS draws 3.4mA and has a phase noise of -88dBc/Hz at 1MHz offset.

10:10 am - Break

20.5

10:25 am

Signal Processing Architectures for Low-Noise High-Resolution CMOS Image Sensors (INVITED PAPER), S. Kawahito, Shizuoka University

In this paper, signal processing architectures for low-noise high-resolution CMOS image sensors are reviewed and discussed. For low-noise signal readout, a column amplifier plays an important role for reducing both the noises due to a wideband output buffer and a pixel source follower. With high amplifier gain, a double-stage noise canceling technique and an advanced signal processing using oversampling techniques effectively reduces the noise due to the pixel source follower. Architectures and topologies for on-chip A/D conversion including pixel parallel, column parallel and serial schemes are discussed. On-chip column parallel analog-to-digital (A/D) conversion is particularly important for low-noise and high-speed signal readout.

20.6

10:50 am

A $1.8\ \text{mm}^2$, 11 mA, 23.2 dB-NF, discrete-time filter for GSM/WCDMA/WLAN using retiming technique, T. Sano, T. Maruyama, I. Yasui, H. Sato and T. Shimizu, Renesas Technology

The discrete-time filtering is suitable for pass band selection and anti-alias filtering. Reduction of large switched-capacitor area is a key issue for the filter. In this paper, we propose the retiming technique and the optimization of unit capacitor to reduce the number of capacitors. The area of the filters is $1.8\ \text{mm}^2$. Noise Figure (NF) and current consumption in GSM mode are 23.2 dB and 11 mA, respectively.

20.7

11:15 am

An Equalized Ultra-Wideband Channel-Select Filter with a Discrete-Time Charge-Domain Band-Pass IIR Filter, A. Yoshizawa and S. Iida, Sony Corporation

An ultra-wideband channel-select filter with equalized pass-band characteristics has been implemented with a $0.13\ \mu\text{m}$ CMOS technology. A discrete-time charge-domain IIR band-pass filter is used to compensate degradation of the 3rd-order continuous-time LC-LPF and the sinc response of the 1st-order charge-domain LPF. Measurements show that the IIR BPF reshapes the pass-band, allowing a 3-dB bandwidth of 500 MHz with a notch at 1 GHz. The filter dissipates 18.8 mW from a 1.2-V supply voltage.

Session 21 – High Performance Processors and Digital Techniques

Fir Ballroom, Wednesday Morning, September 19

Chair: Aurangzeb Khan

Co-Chair: Henry Chang

This session examines processor architectures, design methods, and implementations in 90nm and 65nm. Additional digital techniques are explored in the areas of low power, reliability and emulation-based verification.

8:25 am

Introduction

21.1

8:30 am

Cell Broadband Engine Processor Design Methodology (INVITED PAPER), O. Takahashi, E. Behnen, S. Cottier, P. Coulman, S. Dhong, B. Flachs, P. Hofstee, C. Johnson and S. Posluszny, IBM

The Cell BE design methodology is described which enables high frequency, high performance, power efficient, and area optimized design. It includes a hierarchical design style, clean clock boundary, effective use of non-scan latches, at-speed scan testing, custom design like synthesized macro, fine grained clock gating scheme, and cycle accurate power analysis.

21.2

9:20 am

Implementation of the 65nm Cell Broadband Engine, M. Riley, B. Flachs, S. Dhong, G. Gervais, S. Weitzel, M. Wang, D. Boerstler, M. Bolliger, J. Keaty, J. Pille, R. Berry, and O. Takahashi, IBM, Y. Nishino, Sony Computer Entertainment, T. Uchino, Toshiba America

The first generation Cell Broadband Engine processor introduced the CELL Architecture that consists of nine processor cores fabricated in the 90nm CMOS SOI technology. This paper describes the advances made by moving Cell Broadband Engine design from 90nm CMOS SOI to 65nm CMOS SOI.

21.3

9:45 am

Compact Fault Recovering Flip-Flop with Adjusting Clock Timing Triggered by Error Detection, S. Yasuda and S. Fujita, Toshiba Corporation

We propose novel compact fault recovering flip-flops (CFR-FFs) which can recover timing error and soft error. Two kinds of CFR-FFs are proposed. One is that the clock rises every cycle, and the other is that the clock rises only when data has changed. Error rates were experimentally measured by applying a noise signal to the supply voltage. It is confirmed that the proposed CFR-FFs can highly suppress the errors more than a conventional FF.

10:10 am - Break

21.4

10:25 am

A 2GHz, 7W (max) 64b Power™ Microprocessor Core, D. Murray, J. Burnette, B. Campbell, M. Chung, B. Fernandes, S. Ghosh, R. Goel, G. Hess, H. Huang, Z. Huang, N. Javarappa, P. Kanapathipilai, F. Klass, F. Liu, A. Mehta, Y. Modukuru, N. Nerurkar, A. Radhakrishnan, S. Santhanam, J. Sugisawa, S. Sundar, H. J. Tam, R. Wen E. Wu, J.-C. Yeh, J. Yong, and Z. Zambare, PA Semi, Inc.

The PA6T core is an out-of-order superscalar implementation of the Power Architecture. Power efficiency is achieved through micro-architecture, logic, and circuit optimizations. The processor is fabricated in a 65nm, triple Vt, dual oxide 8M CMOS process. Worst-case power dissipation at 2GHz is 7W.

21.5

10:50 am

Power-Efficient Dual-Supply 64kB L1 Caches in a 65nm CMOS Technology, B. Campbell, J. Burnette, N. Javarappa and V. von Kaenel, PA Semi, Inc.

The 64kB L1 caches on the PA6T-1682M SoC CPU are composed of common data and tag structures fabricated in a 65nm CMOS process and deliver a 1.5 cycle read latency with 32GB/s bandwidth at 2GHz. Several features optimize cache performance and power including power-down safe level shifters, streamlined dual-supply bitslices, fine-grain clock gating, and a centralized tag floorplan.

21.6

11:15 am

Process-Tolerant Low-Power Adaptive Pipeline under Scaled-Vdd, S. Ghosh, P. Batra, K. Kim and K. Roy, Purdue University

We implement a low-power and robust pipeline design methodology suitable for aggressive voltage scaling while maintaining high frequency operations. We isolate the critical paths; make them predictable (by design) and ensure they are activated rarely. At scaled supply (frequency unchanged), possible delay errors (under 1-cycle) are predicted ahead in time and avoided by adaptively stretching the clock period. Test-chip implementation in 130nm process shows 40% power savings with 13% performance loss and ~9.4% area overhead.

21.7

11:40 am

ASIC Design and Verification in an FPGA Environment, D. Markovic, C. Chang, B. Richards, H. So, B. Nikolic and R. Brodersen, University of California Berkeley

A unified algorithm-architecture-circuit co-design environment for dedicated signal processing hardware is presented. The approach is based on a single design description in the graphical Matlab/Simulink environment that is used for FPGA emulation, ASIC design, verification and chip testing. The tool flow propagates up circuit-level performance and power estimates to rapidly evaluate architecture-level tradeoffs. The common Simulink design description minimizes errors in translation of the design between different descriptions, and eases the verification burden. The approach is demonstrated on an ASIC for 4x4 MIMO signal processing.

Session 22 – mm-Wave Systems and Building-Blocks

Pine Ballroom, Wednesday Morning, September 19

Chair: Cicero Vaucher

Co-Chair: John Rogers

This session will present advances in mm-Wave transmitters and receivers. In addition the design of on-chip programmable phase shifters and mm-wave power amplifiers will be addressed.

8:25 am

Introduction

22.1

8:30 am

mm-Wave Silicon ICs: Challenges and Opportunities (INVITED PAPER), A. Hajimiri, California Institute of Technology

Millimeter-waves offer promising opportunities and interesting challenges to silicon integrated circuit and system designers. These challenges go beyond standard circuit design questions and span a broader range of topics including wave propagation, antenna design, and communication channel capacity limits. It is only meaningful to evaluate the benefits and shortcomings of silicon-based mm-wave integrated circuits in this broader context. This paper reviews some of these issues and presents several solutions to them.

22.2

9:20 am

65-nm CMOS, W-Band Receivers for Imaging Applications, K. Tang, M. Khanpour, S. Voinigescu, University of Toronto, P. Garcia, C. Garnier, STMicroelectronics

Two 76-92 GHz receivers, featuring 3-stage cascode LNAs coupled through a transformer to a double-balanced Gilbert-cell mixer and differential DC-5GHz IF buffer, are reported in 65-nm general purpose (GP) CMOS technology. One receiver features a traditional LNA with series-series inductive feedback, while the LNA of the second receiver employs a shunt-series, transformer-feedback cascode stage. Both receivers have a differential down-conversion gain of 12 dB, an input P1dB of -13 dBm, and a double-sideband noise figure of 9-10 dB. They each occupy an area of 550 μ m \times 550 μ m and consume 94 mW. An LO-to-RF isolation of 60 to 59 dB was measured for LO signals in the 80-85 GHz range. The transformer-feedback provides a broader bandwidth input match, lower than -10 dB from 74 to 95 GHz.

22.3

9:45 am

A 4-Channel 24-27 GHz UWB Phased Array Transmitter in 0.13 μ m CMOS for Vehicular Radar, H. Krishnaswamy and H. Hashemi, University of Southern California

An Ultra-wideband (UWB) Variable-Phase Ring Oscillator (VPRO) and Phase-Locked Loop (PLL) architecture for integrated phased-array transmitters is presented. A wideband VPRO operates at half the desired frequency range, and a squarer is used in each channel to cover the $\pm 180^\circ$ phase-shift range completely. A waveform-adaptive, tunable-narrowband design paradigm is introduced that greatly simplifies the design of the UWB blocks. A fully-integrated, 4-channel, 24-27 GHz, phased-array transmitter is implemented in 0.13 μ m CMOS to validate these claims.

10:10 am – Break

22.4

10:25 am

A CMOS 22-29GHz Receiver Front-End for UWB Automotive Pulse-Radars, V. Jain, P. Heydari, University of California Irvine and S. Sundararaman, Avago Technologies

The design of a CMOS 22-29GHz pulse-radar receiver (RX) front-end for ultra-wideband (UWB) automotive radar sensors is presented. Fabricated in a 0.18 μ m CMOS process, the 3mm² RX chip achieves a conversion gain of 35-38.1dB, noise figure of 5.5-7.4dB and input return loss less than -14.5dB in the 22-29GHz band. The phase noise of the constituent QVCO is -107dBc/Hz at 1MHz offset from a center frequency of 26.5GHz. The total dc power dissipation of the RX including LO/output buffers is 131mW.

22.5

10:50 am

An X- and Ku-Band 8-Element Linear Phased Array Receiver, K.-J. Koh and G. M. Rebeiz, University of California, San Diego

This paper presents an 8-element linear phased array receiver adopting RF phase shifting architecture in 0.18- μ m SiGe BiCMOS technology for X- and Ku-band applications. The receiver shows about 20 dB of power gain per channel at 12 GHz with a 3-dB gain bandwidth from 8.5 to 14.5 GHz. The rms gain error is less than 0.9 dB and the rms phase error is less than 6 degree at 6-18 GHz for all the 4-bit phase states. The minimum NF is 3.85 dB at 10-11 GHz and typical input P1dB at 12 GHz is -31 dBm with 170 mA of current consumption from a 3.3 V supply voltage. The overall chip size is 2.2 \times 2.45 mm².

22.6

11:15 am

A 30-40 GHz 1:16 Internally Matched SiGe Active Power Divider for Phased Array Transmitters, J. May and G. Rebeiz, University of California, San Diego

An active 1:16 30-40 GHz power divider was implemented in 0.18 μ m SiGe BiCMOS. The 2 x 2 mm² splitter exhibits 4.5 \pm 1.5 dB total power gain with rms phase imbalance of less than 6 $^\circ$ from 30 to 40 GHz across all 16 channels, consumes 190 mA from a 3.3 V supply, is 15x smaller than an equivalent Teflon-based PCB transmission-line 1:16 power divider, and is the first 1:16 Ka-Band SiGe active power divider.

22.7

11:40 am

A 60 GHz Power Amplifier in 90nm CMOS Technology, B. Heydari, M. Bohsali, E. Adabi and A. Niknejad, University of California Berkeley

A two-stage 60 GHz 90nm CMOS PA has been designed and fabricated. The amplifier has a measured power gain of 9.8 dB. The input is gain matched while the output is matched to maximize the output power. The measured P-1dB =6.7 dBm with a corresponding power added efficiency of 20%. This amplifier can be used as a pre-driver or as the main PA for short range wireless communication. The output power can be boosted with on-chip or spatial power combining.

Session 23 – Methodology and Design for Process Variability Mitigation

Cedar Ballroom, Wednesday Morning, September 19

Chair: Philippe Jansen

Co-Chair: Hamid Mahmoodi

This session addresses different aspects and approaches to mitigate process variability for yield enhancement for nano-scale CMOS technologies. The discussed topics include yield estimation, design/process interaction, and design for yield.

8:25 am

Introduction

23.1

8:30 am

At Tape-out: Can System Yield in Terms of Timing/Energy Specifications Be Predicted? (INVITED PAPER), A. Papanikolaou, M. Miranda, P. Marchal, B. Dierickx and F. Catthoor, IMEC

Process variability is introducing uncertainty in all the system level parametric specifications. Existing variability aware techniques can only capture and model the variations on system timing and leakage power. This paper proposes a framework that can capture variability in the dynamic energy consumption as well. It percolates variability information from semiconductor process to the Register Transfer Level. This enables to capture the application dynamics and provide an accurate estimation of dynamic energy along with leakage and timing.

23.2

8:55 am

Process/Product Interactions in a Concurrent Design Environment (INVITED PAPER), L. Bair, Advanced Micro Devices

The interactions between VLSI processes and the products built in them continue to perplex those who design and those who manufacture semiconductor chips. Predicting, preventing, and minimizing these interactions is compounded by attempts to minimize time-to-market through concurrent process and design development in integrated design and manufacturing environments. Past experience, engineering conservatism, and flexible design techniques enable successful concurrent deep submicron CMOS VLSI designs.

23.3

9:20 am

Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect, Y. Ogasahara, M. Hashimoto and T. Onoye, Osaka University

This paper proposes an all digital measurement circuit called "gated oscillator" for capturing waveforms of dynamic power supply noise. The gated oscillator is constructed with standard cells, and thus easily embedded in SoCs. The performance of the gated oscillator is testified with fabricated test chips in a 90nm process. Characteristics of decoupling capacitance are discussed focusing on channel length and distance, based on supply noise waveforms measured by the gated oscillator.

23.4

9:45 am

An Embedded 8-bit RISC Controller for Yield Enhancement of the 90-nm PRAM, H. Kim, J. Yoo, H.-J. Yoo, KAIST, and K. Sohn, Samsung

An embedded 8b RISC for advanced memories is designed to control, analyze and optimize the memory timing and voltage parameters. The processor-based built-in-selfoptimize(BISO) algorithm is proposed to enhance the memory yield. A test PRAM with the RISC is fabricated in 90nm, 3-metal diode-switch process. By applying BISO, the PRAM margin window increases by 221%. It operates at 100MHz and consumes 28.4mW at 1.0V supply voltage. The embedded RISC enables 100Mb/s/pin read/write throughputs to PRAM.

10:10 am – Break

Session 24 – Advanced Memories

Cedar Ballroom, Wednesday Morning, September 19

Chair : Kenji Noda

Co-Chair: Sreedhar Natarajan

This session covers SRAM alternatives, and describes the evolution of electronically-programmed fuses to enable redundancy.

10:20 am

Introduction

24.1

10:25 am

A 180 Kbit Embeddable MRAM Memory Module, J. J. Nahas, T. Andre, B. Garni, C. Subramanian, H. Lin, S.M. Alam, K. Papworth and W. L. Martino, Jr., Freescale Semiconductor

A 180 Kbit Magnetoresistive Random Access Memory (MRAM) designed for embedding in a 0.28 micron CMOS process has been developed. The memory cell is based on a 1-Transistor 1-Magnetic Tunnel Junction (1T1MTJ) bit cell. The architecture, write driver, and sense amplifier are described. The use of a Test Register to characterize and optimize the memory design is also discussed.

24.2

10:50 am

A 1.0GHz multi-banked embedded DRAM in 65nm CMOS featuring concurrent refresh and hierarchical BIST, D. Anand, J. Covino, J. Dreibelbis, J. Fifield, K. Gorman, M. Jacunski, J. Paparelli, G. Pomichter, D. Pontius, M. Roberge and S. Sliva, IBM

An embedded DRAM macro fabricated in 65nm CMOS achieves 1.0GHz multi-banked operation at 1.0V yielding 584 Gbits/sec. The array utilizes a $0.11\mu\text{m}^2$ cell with 20fF deep trench capacitor and 2.2nm gate oxide transfer gate. Concurrent refresh allows for high availability via a second bank address. At-speed test and repair is accomplished with a new hierarchical BIST architecture. Measured random cycle time exceeds 333MHz at 1.0V with functional operation from 750mV to 1.5V and densities up to 36.5Mbits

24.3

11:15 am

Electrically Programmable Fuse (eFUSE): From Memory Redundancy to Autonomic Chips (INVITED PAPER), N. Robson, J. Safran, C. Kothandaraman, A. Cestero, X. Chen, R. Rajeevakumar, A. Leslie, D. Moy, T. Kirihata and S. Iyer, IBM

Electrical fuse (eFUSE) has become a popular choice to enable memory redundancy, chip identification and authentication, analog device trimming, and other applications. We will review the evolution and applications of electrical fuse solutions for 180nm to 45nm technologies at IBM, and provide some insight into future uses in 32nm technology and beyond with the eFUSE as a building block for the autonomic chip of the future.

Session 25 – Advanced Oscillator Concepts

Oak Ballroom, Wednesday Afternoon, September 19

Chair: Trudy Stetzler

Co-Chair: Nobuyuki Itoh

Oscillators form the fundamental building blocks of all wireless transceivers. Oscillators also play an important role in power efficient frequency dividers. The papers in this session examine the basic trade-offs in oscillator performance and novel low phase noise topologies.

1:30 pm

Introduction

25.1

1:35 pm

Advanced Design Techniques for Integrated Voltage Controlled LC Oscillators (Invited Paper), P. Kinget, B. Soltanian, S. Xu, S.-A. Yu and F. Zhang, Columbia University

25.2

2:25 pm

A 0.5-V 16GHz-20GHz Differential Injection-Locked Divider in 0.18- μ m CMOS Process, H. Zheng and H. Luong, The Hong Kong University of Science and Technology

An ultra-low-voltage (ULV) differential injection-locked (IL) divider topology is presented. By making use of a double-balanced active mixer with transformer feedback (TF) and a TF-VCO, the proposed ULV-IL divider features double-balanced differential-input differential-output, an ultra-low supply voltage comparable to the device threshold voltage, and low power consumption. Fabricated in a standard 0.18- μ m CMOS process and operated at 0.5-V supply, the ULV-IL divider measures an input frequency range from 16.1 GHz to 20 GHz while consuming a total power from 2.75 mW to 4.35 mW. Moreover, two identical proposed ULV-IL dividers with differential inputs are implemented to achieve quadrature outputs with measured IQ sideband rejection of better than -35 dBc.

25.3

2:50 pm

A 1V 4GHz-and-10GHz Transformer-Based Dual-Band Quadrature VCO in 0.18 μ m CMOS, S. Rong and H. C. Luong, The Hong Kong University of Science and Technology

A notch-peak cancellation concept is introduced in transformer-based LC tanks to achieve a dual-band quadrature VCO. Fabricated in 0.18 μ m CMOS process and operated at 1V supply, the QVCO prototype measures a stable dual-band operation from 3.27GHz to 5.02GHz and from 9.48GHz to 11.36GHz. At

4.2GHz and 10GHz, the QVCO measures phase noise at 1MHz offset of -116.3dBc/Hz and -112dBc/Hz, and sideband rejection ratios of 49dB and 47dB while drawing 6mA and 10mA, respectively.

Session 26 – Imagers and MEMS

Fir Ballroom, Wednesday Afternoon, September 19

Chair: Sang-Soo Lee

Co-Chair: Makoto Nagata

This session presents CMOS image sensors for DNA microarrays, electrochemical and fluorescence detection, as well as a high frame rate imager and a MEMS-based system for in-vivo neural imaging.

1:30 pm

Introduction

26.1

1:35 pm

A CMOS Image Sensor for DNA Microarrays, S. Parikh, G. Gulak and P. Chow, The University of Toronto

An image sensor designed with standard 0.18 μm CMOS technology is used to construct a DNA microarray scanner. The detection limit of 4590 fluorophores/ μm^2 is compared with 4.49 fluorophores/ μm^2 of a commercial photomultiplier-tube-based microarray scanner. The performance gap can be reduced by improving optical coupling, mechanical alignment, laser power supply noise, improved circuit noise and an increase in the conversion gain. The CMOS sensor offers multiple-pixels for reduced scan time and an integrated analog-to-digital converter.

26.2

2:00 pm

Active CMOS Array for Electrochemical Sensing of Biomolecules, P. Levine, P. Gong, K. Shepard, Columbia University, and R. Levicky, Polytechnic University

We describe the design of a 4x4 active sensor array for multiplexed electrochemical biomolecular detection in a 0.25- μm CMOS process. Integrated potentiostats sense the current flowing through the on-chip Au electrodes that result from reactions occurring at the chip surface. Preliminary experimental results include cyclic voltammetry of several redox species and application to DNA probe coverage characterization.

26.3

2:25 pm

A CMOS Array Sensor for Sub-800-ps Time-Resolved Fluorescence Detection, T.-C. Huang, K. Shepard, P. Gong, Columbia University, and R. Levicky, Polytechnic University

This paper describes the design of an active CMOS sensor array for fluorescence applications which enables time-gated, time-resolved fluorescence spectroscopy. The 64 x 64 array is sensitive to photon densities as low as 8×10^6 photons/ cm^2 with 64-point averaging and, through a differential pixel design, has a measured impulse response of better than 800 ps. Applications include both active microarrays and high-frame-rate imagers for fluorescence lifetime imaging microscopy.

26.4

2:50 pm

A High-Speed CMOS Image Sensor with On-chip Parallel Image Compression Circuits, Y. Nishikawa, S. Kawahito, M. Furuta, Shizuoka University, and T. Tamura, Photron Ltd.

This paper presents a high-speed CMOS image sensor with on-chip parallel image compression circuits. The chip consists of a pixel array, an A/D converter array with noise canceling function and an image compression processing element array and buffer memories. The image compression processing element is implemented with a 4x4 point Discrete Cosine Transform(DCT) and a modified zigzag scanner with 4 blocks. A prototype high-speed CMOS image sensor integrating the image compression circuits is implemented based on 1-poly 5-metal 0.25- μm CMOS technology. Image encoding using the implemented parallel image compression circuits to the image captured by the high-speed image sensor is successfully performed at 3,000[frame/s].

26.5

3:15 pm

Integration of CMOS and MEMS Technologies in the Development of a Neural Imaging and Interface Device: Showcase of an Emerging Bioimaging Technique, D. Ng, T. Mizuno, T. Tokuda, M. Nunoshita, H. Tamura, Y. Ishikawa, S. Shiosaka and J. Ohta, Nara Institute of Science and Technology

We combine MEMS technology and CMOS image sensors to develop a neural imaging and interface device. Pt electrodes are embedded onto strategic sites on the image sensor for electrical stimulus and recording. On-chip fluorescence imaging is realized by integrating LED chips and coating the device with an excitation light filter. The fully-packaged device demonstrated simultaneous imaging and stimulation inside the brain. We also verified physiologically that the brain is not impaired by the implanted device.

Session 27 – Substrate Noise Modeling; Behavioral Models

Pine Ballroom, Wednesday Afternoon, September 19

Chair: Laurence Nagel

Co-Chair: Gennady Gildenblat

Recent substrate noise models are the subject of the first part of the session. The second part includes applications of behavioral modeling to advanced integrated circuit design.

1:30 pm

Introduction

27.1

1:35 pm

Physical Model for Power Supply Noise and Chip/Package Co-Design in Gigascale Systems with the Consideration of Hot Spots, G. Huang, D. Sekar, A. Naeemi, J. Meindl, Georgia Institute of Technology, K. Shakeri, Cypress Semiconductor

An analytical physical model is derived to predict the first droop SSN noise for non-uniform current switching conditions. The model not only captures the impact of package parameters and the distributed nature of power grid and decap but also addresses the non-uniform current distribution brought by hot spots. A case study shows that both the frequency domain power noise model and the projected peak noise value have less than 1% error comparing with SPICE simulation.

27.2

2:00 pm

Simulation and Modeling of Substrate Noise Generation from Synchronous and Asynchronous Digital Logic Circuits, C. Hanken, J. Le, T. Fiez and K. Mayaram, Oregon State University

An efficient methodology for simulating the substrate noise generated by complex synchronous and asynchronous digital logic circuits is presented. By simulating digital logic at the gate level, the substrate noise generated is used in a transistor level simulation of the sensitive analog blocks. This approach is

shown to be accurate for both traditional CMOS logic and NULL Convention Logic (NCL) by correctly modeling critical gate characteristics. Simulations with different implementations of an 8051 processor core are in good agreement with measurements from a 0.25 μ m CMOS test chip.

27.3

2:25 pm

Chip-Level Substrate Noise Analysis with Emphasis of Vertical Impurity Profile for Isolation, D.

Kosaka, M. Nagata, Kobe University, Y. Murasaka, A. Iwata, A-R-Tec

Slice-and-stack representation of a vertical substrate impurity profile in F-matrix computation captures isolation effects of deep N-wells as well as guard rings in chip-level substrate coupling. It is elucidated that the models of substrate coupling in twin-tub and triple-well designs are dominated by the leakage of Vss noise and capacitive coupling from Vdd noise, respectively, from measurements and analysis of a reference test chip in a 0.18- μ m CMOS p-type bulk technology.

27.4

2:50 pm

Automated Extraction of Model Parameters for Noise Coupling Analysis in Silicon Substrates, B.

Peterson, K. Mayaram and T. Fiez, Oregon State University

An automated process, requiring the fabrication of only a few simple test structures, can efficiently characterize a silicon substrate by extracting the process constants of a Z-parameter based macromodel. The resulting model is used to generate a resistive substrate network that can be used in noise coupling simulations. This process has been integrated into the Cadence DFII environment to provide a seamless substrate noise simulation package which alleviates the need for pre-characterized libraries.

27.5

3:15 pm

Modeling and Simulation of Noise in Closed-Loop All-Digital PLLs using Verilog-A, W. Fergusson,

R. Patel and W. Bereza, Altera Corp.

The modeling and simulation of an all-digital PLL is presented. Verilog-A, owing to its flexibility, is used to create both behavioral and gate-level models used in system-level and circuit-based simulation. The methodology presented allows us to simulate the PLL closed-loop and accurately take into account reference phase noise, DCO phase noise, quantization noise and any excess of it, allowing us to validate our jitter budget for any given application.

3:40 pm – Break

27.6

3:50 pm

Time-Domain Modeling of a Phase-Domain All-Digital Phase-Locked Loop for RF Applications, I.

Syllaios, P. Balsara, University of Texas, and R. Staszewski, Texas Instruments

A new all-digital phase-locked loop (ADPLL) for RF wireless applications has recently been proposed and commercially demonstrated. It replaces conventional phase/frequency detector and charge pump with a time-to-digital converter (TDC). Analog frequency tuning of a VCO is replaced with an all-digital tuning of a digitally-controlled oscillator (DCO). In this paper, we present novel time-domain modeling and simulation techniques of the ADPLL phase detection mechanism. The modeling principles are validated through experimental results.

27.7

4:15 pm

Accurate Modeling of RF Circuit Blocks: Weakly-Nonlinear Narrowband LNAs, J. Croon, D.

Leenaerts and D. Klaassen, NXP Semiconductors

An extensive behavioral model is presented for weakly-nonlinear narrowband LNAs. The electrical transfer, intermodulation, and noise properties are all well described. Performance figures can be predicted for varying source and load conditions. A Verilog-A implementation facilitates cross-platform simulations. The model is compared to transistor-level simulations of a simple textbook LNA and of a state-of-the-art 65nm CMOS LNA in combination with a mixer. Excellent agreements are achieved.

27.8

4:40 pm

Analytical Eye-diagram Model for On-chip Distortionless Transmission Lines and Its Application to Design Space Exploration, M. Hashimoto, J. Siriporn, Osaka University, A. Tsuchiya, Kyoto University, H. Zhu and C.-K. Cheng, University of California, San Diego

This paper proposes a closed-form eye-diagram model for on-chip distortionless transmission lines with intentionally inserted shunt conductance. We derive expressions of eye-opening both in voltage and time, by assuming a piece-wise linear waveform model. The model is experimentally verified. We also apply the proposed model to design trade-off analysis.

GENERAL INFORMATION

LOCATION DoubleTree Hotel
2050 Gateway Place
San Jose, CA 95110
(408) 453-4000
www.doubletree.com

REGISTRATION

Payment of the Technical Session registration fee entitles the registrant to entrance to all Monday-Wednesday Technical Sessions, the Exhibit Hall, Monday's Welcome Reception, Tuesday's Conference Reception, and to one CD ROM of the Conference Proceedings. Hard copy of the proceedings is an additional cost. Single-day registration (Monday, Tuesday, Wednesday) entitles the registrant to that day's events and one CD ROM of the Conference Proceedings. Technical session registration does not include entrance to the Sunday Educational Sessions.

Payment of the Sunday Educational Sessions registration fee entitles the registrant to entrance to the Sunday Educational Sessions, lunch on Sunday, and one copy of the Educational Sessions Workbook. Educational Session registration does not include entrance to the Monday-Wednesday Technical Sessions, the Exhibits or a copy of the Conference Proceedings or CD ROM.

How to Register

Online Registration

To register online for the Technical Sessions and/or Sunday Educational Sessions go to the CICC website at www.ieee-cicc.org. Click on Registration.

Registration by Mail or Fax

To register by fax or mail fill out the registration form in the center of this booklet and fax or mail the form and payment.

Mail the form to:

CICC Conference
19803 Laurel Valley Place
Montgomery Village, MD 20886

OR

Fax the form to: 301-527-0994

Don't register online and by mail or fax –it will result in double billing!

**Online and mail/fax registration forms MUST be received by
Friday, August 31**

After that date please register onsite at the conference.

Make checks payable to CICC 2007 in US dollars on a US bank. We also accept **VISA, MasterCard, American Express and Discover**. Requests for cancellations must be received by September 7, 2007 to qualify for a refund. All cancellations will be charged a \$25.00 processing fee.

Questions on Your Registration

If you have questions on your registration please contact:

By email: cicc@his.com

By phone: 301-527-0900 x 101

By fax: 301-527-0994

Onsite Registration and Advance Registration Badge Pick-Up

The Registration Center, located in the Bayshore Foyer, will be open as follows:

Registration for Sunday Educational Sessions Only

Sunday, Sept. 16 7:00 am - 2:00 pm

Registration for Technical Sessions

Sunday, Sept. 16 2:00 pm - 5:00 pm

Monday, Sept. 17 7:30 am - 5:00 pm

Tuesday, Sept. 18 8:00 am - 5:00 pm

Wednesday, Sept. 19 8:00 am - 3:00 pm

HOTEL ACCOMMODATIONS

The DoubleTree Hotel is located at 2050 Gateway Place, San Jose, California. The hotel has an outdoor swimming pool and exercise facilities. Parking at the Hotel is \$2/hour, maximum \$10/day. The hotel has a complimentary shuttle from San Jose Airport. The hotel is only 1 mile from the San Jose Airport.

The room rate is \$125 for a single or double room. All rooms must be guaranteed with a credit card. To make a hotel reservation call the hotel at (408) 453-4000 or go to the CICC website www.ieee-cicc.org, click on Hotel Reservations, then complete the form.

The cut-off date for the CICC rate is August 24, 2007. To qualify for the CICC rate you MUST make your hotel reservation by the cut-off date. Make certain you tell reservations you are with IEEE CICC.

You will receive a reservation confirmation directly from the hotel. It is the responsibility of each participant to make changes or cancellations directly with the hotel no later than 24 hours prior to scheduled arrival. No refunds will be given by the hotel for changes or cancellations with less than 24 hours notification.

EDUCATIONAL SESSIONS

On Sunday, Sept. 16, the CICC sponsors three Educational Sessions.

These Sessions are:

1. Mixed-Signal SOC Design Methodology
2. High-Speed Serial I/O Design Techniques
3. Low Power Embedded ADC Design

To register, complete the Advance Registration Form for receipt by **August 31**.

WELCOME RECEPTION AND CONFERENCE RECEPTION

Welcome Reception – Mon. Evening, Sept. 11, 5:30 pm - 8:00 pm

Donner Pass Ballroom

The CICC social event this year is the Welcome Reception sponsored by the CICC 2007 Exhibits Committee, held in the Exhibit Hall. All conference attendees are cordially invited! Enjoy the evening by browsing around the exhibit area, talking with the exhibitors' staff, viewing the poster session, seeing old friends and meeting new ones.

Conference Reception – Tues. Evening, Sept. 12, 5:30 pm – 7:30 pm

Donner Pass Ballroom

Join the CICC for a Tuesday night reception for a final visit to the Exhibits and to view the next series of Posters.

CICC LUNCHEON

Tuesday, Sept. 18, 12:15 pm - 1:30 pm

Sierra Ballroom

The CICC Luncheon features an address titled "Growing up with Wires and Batteries" by Paul Brokaw of Analog Devices. Luncheon is not included in the registration fee. Luncheon tickets are available through Advance Registration or onsite at a cost of \$35 per ticket.

CONFERENCE PROCEEDINGS

The proceedings contains papers on each presentation. Technical Session registrants will receive one CD ROM of the Proceedings. Hard copy proceedings will be available at an additional charge and on a "first come-first served" basis. The cost is IEEE member: \$80, Non-member: \$90. After the conference, order the Proceedings through: Single Copy Sales, IEEE Service Center, 445 Hoes Lane, Box 1331, Piscataway, NJ, 08855-1331, Customer Service Department (toll free): 800-678-4333. The IEEE catalogue number is 06CH37753

CICC gratefully acknowledges NXP Semiconductors' sponsorship of this CD ROM.

Additional copies of the CD ROM can be ordered onsite at the conference registration desk, IEEE member: \$80, Non-member: \$90. CD ROMs are not for sale by IEEE after the conference.

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The DoubleTree Hotel is approximately 1 mile from San Jose Airport. There is a complementary hotel shuttle from San Jose Airport to the hotel that runs from 6:00 am to midnight. Call the hotel on the DoubleTree Courtesy Phone outside the baggage area at San Jose Airport.

For passengers flying into San Francisco Airport, the San Jose Doubletree is approximately 33 miles from the airport. Supershuttle Service provides shuttle service from the airport to the hotel. Arrangements can be made at Ground Transportation or by calling (415) 558-8500 for more information. You can also make reservations online at www.supershuttle.com. The cost is approximately \$38.00/one way or \$76.00/round-trip. Taxi service is also available from the airport at an estimated cost of \$75.00.

THINGS TO DO IN SAN JOSE

Visit the San Jose Convention & Visitor's Bureau website at www.sanjose.org for a listing of activities and attractions in the San Jose area. Downtown San Jose, including the Convention Center, is accessible from the DoubleTree Hotel via Light Rail service. The "Metro Road" Light Rail stop is two blocks from the hotel and trains run every 15 minutes and cost \$1.75 one way.

BADGES

Badges are required for admittance to all sessions and the exhibit hall. Please wear your badge at all times while attending the conference so that you will not be delayed entry to a session.

FOR FURTHER INFORMATION CONTACT

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IEEE BMAS CONFERENCE

This year the CICC is co-locating with the IEEE Behavior, Modeling, and Simulation Conference 2007. BMAS will take place September 20 – 21 at the DoubleTree Hotel, San Jose, California.

Visit the BMAS website at www.bmas-conf.org for complete conference information.

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