

An 8Mb 1T1C Ferroelectric Memory With Zero Cancellation and Micro-Granularity Redundancy

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Abstract - New design techniques facilitate a high reliability 1T1C 8Mb ferroelectric random access memory with $0.71\mu^2$ cell operating at 1.5V on a 130nm 5LM Cu process. Zero cancellation increases the cell interrogation voltage by using a non-switching ferroelectric capacitor to remove charge from the bit line that compensates the linear charge from the cell capacitor. A micro-granularity redundancy approach preserves high repair probability for up to 128 single bit failures. Trim data is stored in 2T2C configuration rows for redundancy, reference, regulator and control logic adjustment.

I. INTRODUCTION

Ferroelectric random access memories offer several system performance advantages over competing nonvolatile memories. These advantages include fast write speed, low power consumption and practically unlimited endurance. Recently, FRAM developers have announced the availability of reliable ferroelectric materials manufactured using the area efficient capacitor-on-plug stacked cell and only 2 additional masks over standard CMOS processing[1]. FRAM now has the potential to make significant inroads into multi-megabit standalone and embedded memory applications. We have designed and fabricated an 8Mb FRAM incorporating features attractive to system designers and employing design techniques that maximize product reliability. This paper summarizes the design and discloses some of the related design innovations.

II. EXTERNAL FEATURES

The 8Mb FRAM device responds to asynchronous SRAM signaling and can replace existing asynchronous SRAM and pseudo-SRAM devices. The device operates from an external supply of 2.7V to 3.6V and supports all asynchronous SRAM features including address transition detection and late writes. Its 512Kx16 interface with separate upper and lower byte select signals allows the device to also act as a 1Mx8 memory. Like asynchronous SRAM, the address access time matches the cycle time, in this case 60ns. While a previous design on the same technology demonstrated a sub-35ns cycle time[2], other considerations superseded speed for this product. These include a larger capacitor area for improved signal margin combined with the desire to minimize plate driver area and

local undershoot/overshoot. Asynchronous access support also adds some time overhead. A fast column access mode can return the average cycle time to below 35ns. Four data words share a page, and movement to any other word in the same page takes only 25ns.

At the maximum operating frequency, the device draws under 15mA active current. The 1.5V core power supply regulator draws approximately 100uA ready standby current which can be reduced to below 5uA in sleep mode. The device monitors the external power supply and prevents memory access if the supply falls too low. Fig. 1 depicts the operating modes of the device and the triggers for moving from one mode to the next. Power-up and wakeup utilize the same initialization sequence which takes less than 250us. Standby current and wakeup time reduction are areas of future development.

III. DESIGN OVERVIEW

Fig. 2 illustrates the construction of the 8Mb FRAM device. Two 4Mb “blocks” surround the “spine”. Each block contains eight 512Kb “sections” made up of sixteen 32Kb “segments”. Area saving layout techniques include back-to-back plate group drivers and shared sense amplifiers as shown in Fig. 3. The sense amplifiers below the active segment serve the even columns while those above the active segment serve the odd columns. Each plate group (see [3]) serves 32 word lines except for the last plate group which also accesses 4 redundant word lines and 2 configuration word lines.

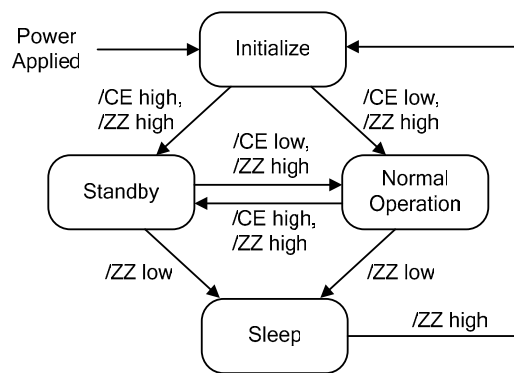


Fig. 1 Simplified Operating Mode Diagram

Standalone Area
16.8 mm²

Embedded Area
< 12 mm²

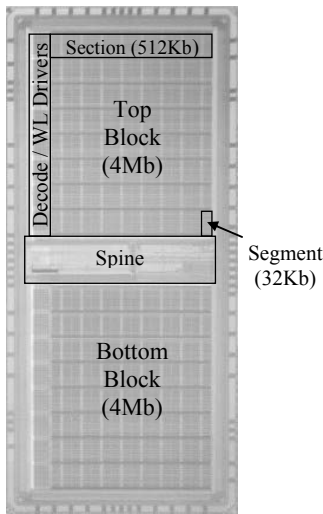


Fig. 2 Annotated Die Photograph

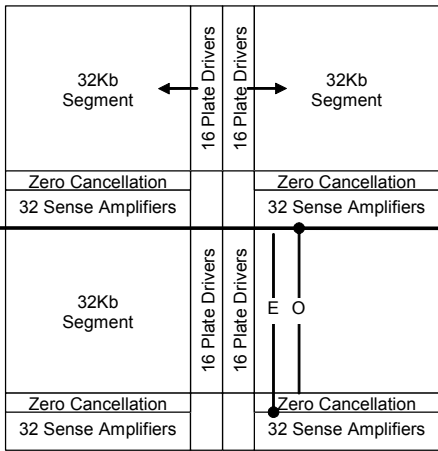


Fig. 3 Segment Layout Detail

TABLE I
CHIP DIMENSION CONTRIBUTIONS

| Height | | Width | |
|--------------------|-------|-------------------|-------|
| Total | 6060u | Total | 2770 |
| Array + Dummy | 64.7% | Array + Dummy | 57.2% |
| Sense Amp | 12.8% | Pads and Cap | 20.6% |
| Pads and Cap | 9.7% | WL Drivers | 9.5% |
| Spine | 8.5% | PL Drivers | 8.2% |
| Zero Cancellation | 1.7% | Redundant Columns | 3.5% |
| LMUX | 1.3% | Substrate Ties | 0.6% |
| Redundant Rows | 0.5% | Routing Allowance | 0.4% |
| Twist Rows | 0.5% | | |
| Configuration Rows | 0.3% | | |

Table I lists the relative contributions to the chip height and width. The embedded area estimate provided in Fig. 2 is derived by removing the “Pads and Cap” contributions and allows more direct comparison to previously published embedded array areas.

The data path design shown in Fig. 4 (top block) exploits the 5 metal levels available by running local IO (“LIO”) lines vertically in the 4th metal layer. Each LIO provides connectivity to 8 even columns and 8 odd columns.

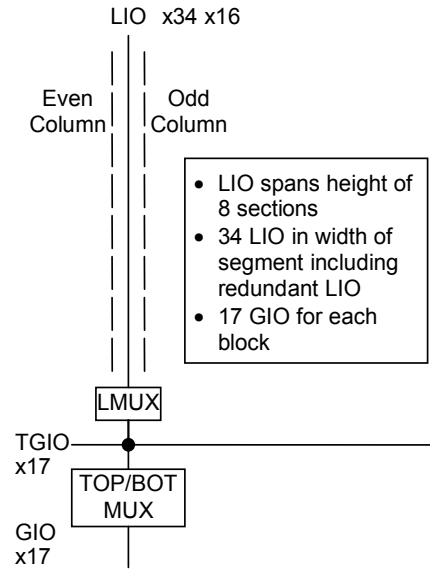


Fig. 4 Data Path Design Including Top Block

This even/odd sharing of LIO lines halves the number of LIO lines and relaxes the LIO pitch. An “LMUX” circuit determines which LIO gets mapped onto the top global IO (“TGIO”) line. The top and bottom blocks have separate GIO busses in order to relieve routing congestion in the spine area. The top block is depicted in Fig. 4, and the LIO and GIO counts include redundancy. The redundancy circuitry controls which 16 of the 17 available GIO lines are connected to the external DQ signals.

IV. ZERO CANCELLATION

The voltage applied to cell capacitors influences both the “same state” and “opposite state” retention performance of ferroelectric materials, especially below the saturation voltage of the material[4]. Fatigue of ferroelectric materials reduces the charge available for switching at a given voltage, but interrogation at higher voltages can recover otherwise lost signal[5]. Although write operations always apply the full supply voltage across the cell capacitor, the read interrogation voltage in conventional FRAM designs falls below the supply voltage due to voltage division between the cell capacitor and the parasitic capacitance of the floating bit line.

One proposed method of increasing the interrogation voltage involves actively holding the bit line at ground during sensing[6]. This approach achieves the goal of increased interrogation; however, the circuit implementation of the bit line ground sensing technique is cumbersome, requiring several negative voltages and new timing signals.

Plate line boosting is another means of increasing the read interrogation voltage[7]. Plate boosting, however introduces two design challenges. First, the plate line load varies depending on the data state of the bits accessed by the plate line, and this complicates boost circuit design. Second, adding boost circuitry to plate drivers can significantly impact chip area. Conventional FRAM arrays generally show greater

sensitivity to circuitry added in the column direction than in the row direction.

Our 8Mb device employs a new technique called zero cancellation to maximize the interrogation voltage. Contrary to plate boosting in which a boost capacitor pushes charge onto a floating plate line, zero cancellation occurs when a capacitor pulls charge off the floating bit line. Fig. 5 illustrates two memory cells adapted to pull charge off the two bit lines in a column, and Fig. 6 explains the timing sequence of zero cancellation in the context of up-down sensing. In the ideal case, the charge pulled off the bit line by the zero cancellation capacitor exactly cancels out the charge pushed onto the bit line by a cell capacitor storing a non-switching (i.e. zero) state. Although perfect zero cancellation will not always occur, the circuit will achieve the goal of increasing interrogation voltage for both non-switching and switching capacitors.

In Fig. 6 the accessed cell transistor connects to BL and the reference (REF) drives onto BLB. The zero cancellation circuit requires initialization at the beginning of the cycle. The existing bit line precharge devices hold BL low while ZCWL and ZCPL go high. The normal cycle can commence once ZCPL has settled at the supply voltage and BL has recovered to ground. The WL rises to access the active row followed by PL rising to interrogate cells in the active segment. With ZCWL high and ZCPL held at a fixed level the zero cancellation capacitor adds some capacitance to the BL. Next, the ZCPL driver pulls ZCPL low which actively removes charge from the bit line and slows the PL rising edge. The PL continues driving to the supply voltage, and the voltage across the cell capacitor increases as BL falls and PL rises.

ZCPL returns high after the zero cancellation circuit establishes the peak interrogation voltage. This accomplishes two things. First, it eliminates potential offsets introduced by process or temperature variations in the zero cancellation capacitors. Second, it raises the bit line voltage prior to the PL falling edge to prevent BL from coupling negative. The ZCPL rising edge dumps charge back onto PL resulting in a momentary 100mV PL overshoot.

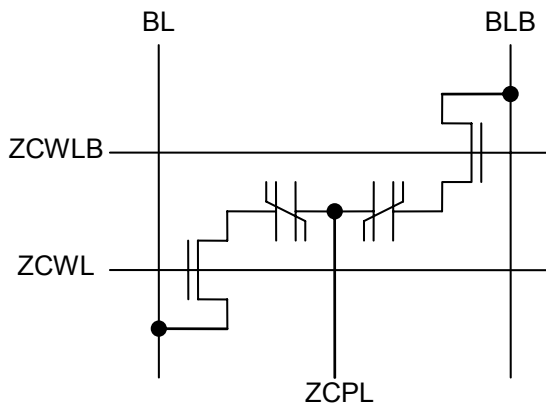


Fig. 5 Zero Cancellation Circuit

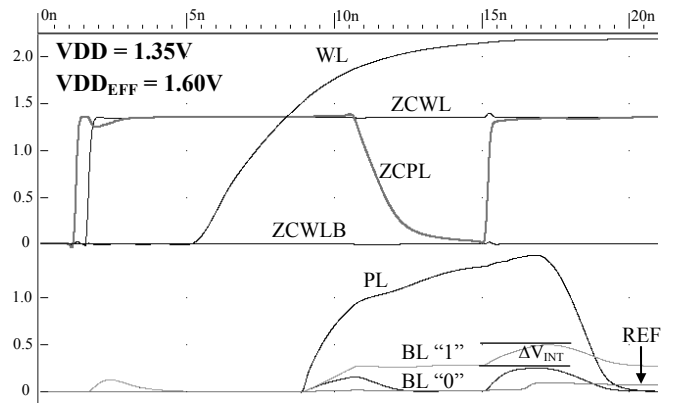


Fig. 6 Zero Cancellation Simulation

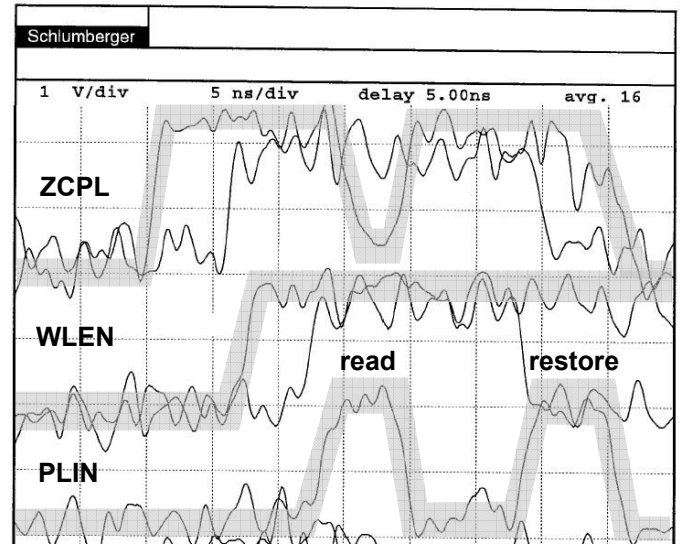


Fig. 7 E-beam Timing Measurements

The difference in voltage on BL "1" from when ZCPL is low to when ZCPL returns high provides an estimate of the increase in interrogation voltage labeled ΔV_{INT} in Fig. 6. The small PL overshoot does result in a slightly high estimate for ΔV_{INT} , but the advantage of zero cancellation can be clearly seen. For ferroelectric material with high linear charge contribution (e.g. capacitor thickness at low end of process limits) zero cancellation increases the interrogation by over 150mV. If zero cancellation were not used, a VDD level of 1.60V would be required to produce the same "1" interrogation. Furthermore, the reliability improvement of this 18% increase in effective VDD during reads is achieved without raising the fatigue-inducing write voltage.

Fig. 7 shows e-beam measurements of select timing signals within the control logic of the fabricated 8Mb memory. The ZCPL, WLEN (word line enable) and PLIN (plate line timing input) signal envelopes are shaded for clarity. The ZCPL low pulse during the "read" plate pulse is evident in Fig. 7. The internal read operation is complete within 35ns for the default timing. The timing can be further contracted by modifying nonvolatile control registers.

V. MICRO-GRANULARITY REDUNDANCY

The 8Mb device includes three types of redundancy, namely row redundancy, column redundancy and micro-granularity redundancy. Each section supports two row repairs and each repair replaces two rows. All sections share the same row repair programming resources which requires full section + row address matching. The device only supports 16 of the 32 possible row repairs in order to reduce the required register area without significantly compromising repair probability.

Four redundant columns reside in each segment with one redundant column dedicated to a group of 16 columns in the same data word. All segments share the same column repair programming resources which requires full section + segment + word address matching and failed IO encoding. The configuration area includes sufficient column repair registers to use 32 of the 1024 redundant columns. Beyond 32 repairs the probability of further column repair steeply declines, and performing additional column repairs would have little impact on product yield.

The third type of redundancy enables 128 additional repairs to individual bit pairs. This repair technique is named micro-granularity redundancy because the repair element is only 2 bits. Micro-granularity redundancy takes its repair elements from redundant columns by performing a repair only when both column and row-pair addresses match. Only the desire to limit the area consumed by repair programming resources limits the number of bit-pair repairs to 128. The use of such small repair elements preserves a high probability for use of all 128 repairs.

VI. FRAM CONFIGURATION

Several aspects of device operation can be adjusted after fabrication. Programmable features include core and WL supply regulator values, memory reference voltage, a global speed trim and the three types of redundancy previously discussed. The device also allows post-fabrication adjustment of signal order and timing in the control circuitry. The configuration information resides in 2T2C FRAM configuration rows located in each section. Addition of the configuration rows incurs a negligible area impact as shown in Table I above.

At power-up, a configuration load controller accesses more than 4Kb of data in the configuration rows and transfers this data into volatile registers located within the circuitry that uses the programming data. The configuration load controller, synthesized from behavioral code and auto-routed using a standard cell library, activates two configuration word lines simultaneously and disables the reference circuitry to achieve 2T2C access of the configuration data. This approach maximizes the reliability of the configuration data and allows FRAM configuration of the memory reference value necessary for 1T1C operation.

Redundancy programming bits consume the bulk of the configuration data. To reduce the probability of defective bits in the configuration row leading to false repairs, two repair enable bits must be set to engage a repair. A special test mode

provides normal memory access to all configuration row bits. A defective bit in a redundancy programming area disqualifies that repair register; however, the interchangeable nature of all repairs of the same type prevents such a failure from disabling the entire chip.

VII. MEASUREMENT RESULTS

The 8Mb FRAM design has been fabricated on a 130nm 5LM Cu process, and functionality has been verified. Internal access times have been measured below 35ns as previously shown in Fig. 7. All three types of redundancy have been confirmed to successfully repair row, column and single bit failures.

VIII. CONCLUSION

We have presented the design of an 8Mb FRAM enhanced by zero cancellation, micro-granularity redundancy and FRAM configuration. Zero cancellation increases the capacitor interrogation voltage while consuming minimal silicon area. Flexible redundancy efficiently improves product yield and reliability by enabling removal of 128 defective or weak bits, 32 defective columns and 16 defective row pairs. FRAM configuration rows consume little area and support over 4Kb of configuration data, most of which programs the redundancy.

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