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Welcome from the CICC Committee

Welcome to the 26th annual Custom Integrated Circuits Conference, CICC 2004. Noteworthy events for this year include a keynote presentation by Dr. Chenming Hu, Chief Technical Officer, TSMC, a conference luncheon with guest speaker, Dr. Frederic Zenhausern, Director, Applied Nano-Bioscience Center, Arizona State University, an expanded technical program with 29 technical sessions, three evening panels, and several social events. The CICC is the leading international conference for integrated circuit development where first time advancements are published. CICC provides a unique forum for all individuals involved with IC development to meet and share information about the most recent advances in system architectures, circuits, computer-aided design, and process technology. CICC's goal is to offer attendees a total educational experience balanced between paper presentations, exhibits, panels, tutorials, and interesting networking events. You are cordially invited to participate in CICC 2004, located in Orlando, Florida, at the Caribe Royale Resort.

Larry Starr
General Chair

The conference starts with three educational sessions on Sunday, October 3. These sessions are taught by practicing experts working at the leading edge of their fields. The topics for these sessions are: Advanced RF: From Devices to Systems, Advanced Data Converter Design Techniques, and High-Performance and Low-Power Microprocessor Design Strategies.

Trudy Stetzler
Conference Chair

On Monday morning, the technical program begins with Dr. Chenming Hu's keynote presentation titled "CMOS for One More Century?" which promises to provide a lively opening for the technical program..

As always the technical sessions are highlighted by invited and tutorial papers presented by leading experts from the industry and academia. This year, more than 376 technical papers were submitted, of which 146 were selected and organized into 29 sessions. These high quality and informative papers address topics including: Wireless & Wired Communications, Analog, Custom & Low Power Circuits, SoC/SiP and IP Design and Management, Simulation & Modeling, Signal & Data Processing, Embedded Memories, Programmable Devices, Fabrication, and Test & Reliability. Again this year's

Henry Chang
Technical Program Chair

CICC has an Emerging Technologies session which features very interesting invited papers on a wide range of topics.

On Monday afternoon the Exhibitor Preview Sessions kick off the opening of the Exhibits Hall. Here many of our Exhibitors will present overviews of new products and services. During the Monday evening Exhibitors' Reception you will find refreshments and professional networking at its very best! As always, our exhibits area will include booths and software demonstrations from prominent corporations in the industry.

You will not want to miss this year's conference luncheon. Our honored guest speaker, Dr. Frederic Zenhausern, will give a presentation on "The Impact of Nanoscale Science on Life Sciences and Medicine", which will be a fascinating and educational experience.

On Tuesday evening, three spirited panel discussions are scheduled featuring experts who are sure to offer strong opinions on the three topic areas: "MEMS and Nanotechnology – Hot or Hype?"; "Are ASICs Dying because of FPGAs and the Price of Software?"; and "SOC vs. SIP, Are We Putting Too Much on One Chip?"

We extend our thanks to all the authors who spent many hours on the preparation of their submitted papers. We also wish to thank the CICC Technical Program Committee and our dedicated conference staff for all of their hard work and support. Their diligent efforts keep CICC as the best place to discover the latest in integrated circuit innovations, to hear the newest product announcements, and to debate the most effective business strategies. See you in Orlando!



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EDUCATIONAL SESSIONS

Sunday, October 3

Chairperson: Doug Garrity, Freescale Semiconductor, Inc.

Ed. Session 1 - Advanced Data Converter Design Techniques

Grand Caribbean Ballroom V, Sunday, October 3

Organizer: Pat Rakers, Freescale Semiconductor, Inc.

Co-Organizer: Don Thelen, AMI Semiconductor, Inc.

E1-1 Introduction to Sigma-Delta Data Converters

8:00 – 9:50 Matt Miller, Freescale Semiconductor, Inc.

As IC process technologies have progressed, noise-shaping data converters, already known for their superior linearity performance, have steadily overtaken wider bandwidth applications previously dominated by Nyquist-rate data converters. This talk will start with the fundamental concepts of noise-shaping converters and also cover some of the more recent architectural innovations that have led to the dominance of the sigma-delta data converter as the choice for a wide variety of high resolution-bandwidth applications including wireless receivers. A brief case study of a multi-bit sigma-delta ADC design for a receiver application will help to illuminate some of the key considerations involved in noise-shaping data converter circuit design.

E1-2 Continuous-Time Delta-Sigma ADCs

10:10 – 12:00 Kathleen Philips, Philips Research

Most of present-day delta-sigma ADCs are time-discrete, yet the interest in continuous-time converters has grown rapidly. After a brief introduction on delta-sigma fundamentals, differences between continuous-time and discrete-time implementation are explained. Continuous-time designs have the capability of lower noise (no kT/C) and higher conversion bandwidth than discrete-time implementations. Several examples show that power consumption (normalized to performance) of continuous-time delta-sigma is amongst the lowest reported for data converters. We analyze design challenges like sensitivity to parameter spread, jitter, excess loop delay, memory effects, etc. and present -or refer to- some solutions. Finally, some advanced application examples exploiting the specific characteristics of the time-continuous implementation are discussed.

E1-3 Device Mismatch for Data Converter Design

1:00 – 2:50 Patrick Drennan, Freescale Semiconductor, Inc.

Device matching is the heart of precision analog design. Ironically, the significance of analog has grown more prominent in the "digital" age, due, in part, to data converters. Mismatch variance is inversely proportional to device area, which means that well matched devices come at the expense of larger die, parasitic capacitance and power consumption. Even more expensive, advanced techniques such as laser trimming, memory stored mismatch correction, and mismatch shaping do not lessen the desire for the best intrinsically matched devices. A physical description of mismatch variation will establish the foundation for this presentation. We'll walk through the evolutionary steps of mismatch model development and discuss how mismatch fits into the big picture of statistical device variation. The majority of the presentation will approach mismatch from the design perspective, concentrating on MOSFETs, capacitors, and resistors. This presentation will discuss device sizing, bias dependencies, metal routing over devices, gradient effects, gate protect diodes, dummy devices, and measurement and characterization issues.

E1-4 Digitally Assisted Analog-to-Digital Converters

3:10 – 5:00 Bernhard Boser, University of California, Berkeley

The continued reduction of integrated circuit feature sizes and commensurate improvements in device performance are fueling the progress to higher functionality and performance. For example, over the last 15 years, microprocessor performance has increased over one hundred fold. In the same time frame, analog circuit performance increases much more slowly. For example, the power/resolution figure-of-merit of ADCs improved only by a factor ten. Of the many reasons for this disparity between analog and digital circuit advances, accuracy requirements stand out as a critical constraint in most analog circuits that is virtually absent in digital designs. Typical solutions such as high-gain feedback loops come at a power and performance penalty that is likely to increase with further supply voltage and technology scaling. Digitally assisted analog circuits avoid these tradeoffs by moving some of the analog circuit challenges to the digital domain. Specifically, analog circuit linearity requirements are relegated to a digital postprocessor that identifies and corrects distortion in the analog domain. We will discuss the benefits of digital assistance in the context of pipelined ADCs and give examples for system identification and correction techniques.

Ed. Session 2 - Advanced RF: From Devices to Systems

Grand Caribbean Ballroom VI, Sunday, October 3

Organizer: Larry Nagel, Omega Enterprises

Co-Organizer: Johan Van Der Tang, Eindhoven University of Technology

E2-1 Parasitic-Aware RF Circuit Synthesis

8:00 – 9:50 David Allstot, University of Washington

RF circuit synthesis techniques based on particle swarm optimization and adaptive simulated annealing with tunneling are described, and comparisons of parasitic-aware designs of an RF distributed amplifier and a nonlinear power amplifier are presented. Synthesized in 0.35 μ m digital CMOS using a single 3.3V power supply, the designs provide 8dB gain and 8GHz bandwidth for a four-stage distributed amplifier, and 1.2W output power with 55% drain efficiency at 900MHz for a three-stage power amplifier. A standard circuit simulator, HSPICE or SPECTRE, embedded in an optimization loop is used to evaluate cost functions. The proposed design and optimization methodology is computationally efficient and robust in searching complex multi-dimensional design spaces.

E2-2 Modeling and Simulation Issues in Phase-Locked Systems

10:10 – 12:00 Behzad Razavi, University of California, Los Angeles

Passive and active device models for PLL design; PLL modeling for fast simulation; simulation of phase noise and jitter; bang-bang loop modeling issues; modeling and simulation of clock and data recovery circuits; behavioral versus transistor-level modeling.

E2-3 Advanced Analysis Methods and Simulation Tools for Noise in VCOs and PLLs

1:00 – 2:50

Jaijeet Roychowdhury, University of Minnesota

Amit Mehrotra, Berkeley Design Automation and University of Illinois, Urbana-Champaign

This tutorial will describe recent advances in phase noise and timing jitter prediction, with emphasis on their use and benefits in mixed-signal/RF design, including examples and case studies. The goal of this tutorial is to inform the audience about the best hand-analysis methods and simulation tools available

today for noise and jitter phenomena in oscillators and PLLs. The following topics will be covered:

- LC and ring oscillator operation: basics
- Perturbation analysis of oscillators
- Phase noise and timing jitter in oscillators: intuition and equations
- Analytical perturbation/noise formulae for LC and ring oscillators
- Injection locking in oscillators
- Power/ground noise: effect on oscillator jitter
- PLL jitter and noise
- Phase noise and jitter: tools, examples, case studies

E2-4 RF System Design Tools and Technology Tradeoffs

3:10 – 5:00 Piet Wambacq, IMEC, Belgium

RF systems nowadays consist of clever architectures, often with complicated interactions between analog and digital, which are either wanted (e.g. compensation algorithms, feedback loops) or unwanted (e.g. substrate noise coupling). To enable an optimal design, it must at least be possible to simulate these architectures. However, at the system level, circuit-level issues play a more dominant role for RF and analog circuits than for digital circuits. Hence, it is desirable to have an idea at the system level of the performance and power consumption of the different RF circuits in the complete system. This lecture discusses how RF systems can be simulated efficiently at the system level using accurate high-level models of the analog and RF blocks, possibly in combination with digital parts, in order to study e.g. digital compensation techniques. Further, the analysis and simulation of substrate noise coupling is studied and comparisons between simulations and measurements are discussed. Finally, an approach is presented that allows for a quick assessment of performance and power consumption of a given circuit topology as a function of technology.

Ed. Session 3 - High-Performance and Low-Power Microprocessor Design Strategies
Grand Caribbean Ballroom VII, Sunday, October 3

Organizer: Un-Ku Moon, Oregon State University

Co-Organizer: Steffen Rochel, Cadence Design Systems

E3-1 Low-Power Design Challenges and Techniques

8:00 – 9:50 Lawrence T. Clark, University of New Mexico

The tutorial describes design techniques for limiting both standby (leakage) and active power. The tutorial begins with the impact of transistor scaling on transistor leakage and design techniques to address the resulting standby power. Circuits applying reverse body bias, as well as the use of shadow latches will be described. The application and the efficacy of low power modes, their power penalties, latencies, and limitations will be discussed. Techniques and prospects for managing "active" leakage, that is, the leakage components when an IC is not in a standby state will also be described. The tutorial will then discuss design techniques for limiting active (circuit-switching) power. Practical application of voltage scaling, dynamic voltage scaling, and circuit limitations to low voltage operation will be reviewed. The use of pulse-clocked latches simulating master-slave flip-flops and clock gating to limit sequential circuit power will be described, with examples from real designs. The power impact of architecture and micro-architectural choices will be discussed. The tutorial will conclude with a summary of the proposed techniques, their relative benefit vs. design difficulty and prospects for future low-power ICs.

E3-2 High-Speed Arithmetic and Logic Technologies for Beyond 65nm: Challenges and Opportunities

10:10 – 12:00 Ram Krishnamurthy, Intel Corporation

As traditional CMOS technology scaling becomes difficult beyond 65nm node, new challenges arise for achieving high-performance at low-power and low-cost

across all design platforms: from general-purpose microprocessors/DSPs to dedicated ASICs to entire analog+digital systems-on a-chip. This tutorial discusses the primary sub-65nm scaling issues and trends, and outlines some of the new paradigm shifts necessary for arithmetic and logic designs to overcome these barriers. Design perspectives from the architecture, circuit design, and tool-flow standpoints to enable high-performance and low-power operation are described. Static and dynamic supply scaling, multi-supply and multi-threshold optimization techniques, sleep transistor techniques and their tradeoffs are discussed for switching and leakage energy reduction. High-speed dedicated accelerators and arithmetic building blocks for enabling high MOPS/W on specialized DSP tasks are also outlined. Novel dynamic bit-line techniques are presented to combat poor leakage-tolerance and parameter variation-tolerance of large-signal cache and register file arrays. Further, new full-rail and low-swing single rail on-chip interconnect methodologies and associated accurate RLC optimization techniques are studied for overcoming the worsening global on chip interconnect delay scaling trend.

E3-3 Issues for Memories Embedded in Processors

1:00 – 2:50 Betty Prince, Memory Strategies International

The tutorial discusses various issues for the RAM and non-volatile memories required in microprocessors and microcontrollers. The functions and types of conventional memories used in processors will be reviewed, followed by a discussion of types and advantages or disadvantages of specialty memories embedded in processors such as P-SRAM, single-poly Flash and scaled flash such as SONOS and silicon nanocrystal gates. Various emerging memories targeted for embedding in processors will be discussed such as eMRAM, eFeRAM, SESO, STTM, Capacitorless DRAM, etc. along with projected advantages and disadvantages including cost, speed, power, and CMOS logic compatibility. Issues discussed will include: cost adders over standard/ high performance CMOS logic, high voltage requirements, speed and power issues, redundancy and error correction issues, causes and potential solutions for soft errors, and test.

E3-4 SOI Technology Design Challenges and Solutions

3:10 – 5:00 Rajiv Joshi, IBM Research Division

Front and back end technologies of VLSI circuits continue to evolve. Novel device structures drive the front-end roadmap while copper and low-k dielectric drive the back-end roadmap. Recently silicon on insulator (SOI) has emerged as a technology for mainstream digital applications as the bulk silicon technology is approaching scaling limits rapidly to improve the performance even further. The talk will describe various SOI technologies and will give the perspective of the impact on circuit performance. The advantages of SOI such as reduced source-to-drain resistance and dynamic threshold voltages, which result in higher performance; compatibility with the bulk CMOS processing will be compared with its cons. These include the floating body effect in partially depleted device, which can accumulate or lose charges. This causes high device leakages during standby or in the high temperature burn-in conditions. The amount of charge in the body depends on the initial conditions of source, drain and gate of the device. This results in variable body potentials and dynamic threshold voltages which cause variable device delays known as "history effect". Such SOI specific issues pose multitudes of design challenges which will be described along with the tooling issues. Other design concerns such as inter or intra macro timing problems, race conditions, high leakages/power and reduced noise margins will be discussed. Further the talk illustrates asynchronous circuit styles (e.g. self resetting CMOS) in the light of SOI effects. Achieving acceptably low leakages is a technology challenge. Scaling oxide thickness results in increased gate-to-substrate tunneling which also affect circuit performance. The impact of such effect for SOI will be analyzed. The self-heating effect due to difference in thermal resistances of Buried oxide and Silicon layer in SOI is significant. Finally the talk will analyze the effect of temperature on performance using 3-D thermal analysis.

EXHIBITS

CICC once again combines its outstanding technical program with a variety of exhibitors. Exhibits will include displays and demonstrations by semiconductor manufacturers, software tool suppliers, design service houses, and leading electronics industry publications. The Exhibit Hall will be the site for Monday's Exhibitors' Reception and Tuesday evening's Happy Hour.

Grand Caribbean Ballroom I and II Monday, October 4

2:00 pm - 7:00 pm – Exhibits Open
1:00 pm - 2:00 pm Exhibitor Preview Session
5:30 pm - 7:00 pm Exhibitors' Reception

Tuesday, October 5

2:00 pm - 7:00 pm – Exhibits Open
5:30 pm - 7:00 pm Happy Hour

EXHIBITORS' PREVIEW SESSIONS

Monday, October 4, 1:00 pm - 2:00 pm
Boca III and IV Rooms

TECHNICAL SESSIONS

Monday, October 4 - Wednesday, October 6

Session 1 – Keynote Presentation Grand Caribbean IV, Monday, October 4

8:00am Welcome/Opening Remarks
Awards Presentations
Keynote Speaker Introduction
Larry Starr, General Chairman

8:20am KEYNOTE ADDRESS
“CMOS for One More Century” Dr. Chenming Hu, Chief
Technology Officer, TSMC.

It is not too early to search for the post-CMOS technology. Ideally, the new technology would have an architecture that requires only near neighbor communication to rid the delay/noise of global interconnects, greatly reduced power consumption, low cost, and ability to perform functions now provided by CMOS. If a more competitive technology than CMOS cannot be found, CMOS may have to serve the world's need for intelligent devices and communication through this century. Can CMOS answer the call to duty?

Dr. Hu is on leave from UC Berkeley, where he is TSMC Distinguished Professor of Electrical Engineering and Computer Science. His research area is microelectronic devices and technologies. He has authored or co-authored five books and over 750 research papers. He leads the development of the BSIM transistor model for CMOS circuit simulation. BSIM is the industry standard for IC simulation and is used in the design of most ICs worldwide. He co-developed FinFET. In 1997 Dr. Hu received the IEEE Jack A. Morton Award for contributions to MOSFET reliability physics. In 1999, he received the DARPA Most Significant Technological Accomplishment Award for FinFET, In 2002 he received the IEEE Solid State Circuits Field Award “for SDIM3 modeling and development work.”



Session 2 – Advanced MOSFET Modeling
Grand Caribbean IV, Monday Morning, October 4

Chair: Larry Nagel Co-Chair: Colin McAndrew

RF and mixed-signal design continues to depend critically on the availability of accurate and realistic device models. This session contains four papers on new developments in MOSFET models, including a non-quasi static MOSFET model, models for accurate distortion analysis, the next generation BSIM model, and a model that reflects random-dopant variations in MOSFETs.

10:00 am Introduction

10:05 am A Robust Large Signal Non - Quasi-Static MOSFET Model for Circuit Simulation, H. Wang and G. Gildenblat, The Pennsylvania State University, University Park, PA
2-1

10:30 am RF Distortion Analysis with Compact MOSFET Models, P. Bendix, P. Rakers*, P. Wagh*, L. Lemaitre*, W. Grabinski*, C. McAndrew*, X. Gu, G. Gildenblat**, LSI Logic, Milpitas, CA,*Motorola, Schaumburg, IL, **The Pennsylvania State University, University Park, PA**
2-2

10:55 am The Next Generation BSIM for Sub-100nm Mixed-Signal Circuit Simulation, X. Xi, J. He, M. Dunga, C.-H. Lin, B. Heydari, H. Wan, M. Chan, A.M. Niknejad, C. Hu, University of California, Berkeley, CA
2-3

11:20 am Estimation of Delay Variations Due to Random-Dopant Fluctuations in Nano-Scaled CMOS Circuits, H. Mahmoodi-Meimand, S. Mukhopadhyay, and K. Roy, Purdue University, West Lafayette, IN
2-4

Session 3 – High-Speed Serial Links
Grand Caribbean V, Monday Morning, October 4

Chair: Kumar Lakshmikummar Co-Chair: Jafar Savoj

This session highlights the latest advances in high-speed serial links, employing signal processing techniques and novel circuit topologies to improve transceiver performance for low-bandwidth and low-power environments.

10:00 am Introduction

10:05 am A 1.5V 20/30 Gb/s CMOS Backplane Driver with Digital Pre-Emphasis, P. Westergaard, T.O. Dickson and S.P. Voinigescu, University of Toronto, Toronto, Ontario, Canada
3-1

10:30 am 10+ Gb/s 90nm CMOS Serial Link Demo in CBGA Package, S. Rylov, S. Reynolds, D. Storaska*, B. Floyd, M. Kapur, T. Zwick, S. Gowda, M. Sorna*, IBM T.J. Watson Research Center, Yorktown Heights, NY, *IBM Microelectronics Division, Hopewell Junction, NY
3-2

- 10:55 am 3-3 A 4.8-6.4 Gbps Serial Link for Back-Plane Applications using Decision Feedback Equalization,** *V. Balan, J. Caroselli, J.-G. Chern, C. Desai, and C. Liu, LSI Logic Corporation, Milpitas, CA*
- 11:20 am 3-4 A Low Power Capacitive Coupled Bus Interface Based on Pulsed Signaling,** *J. Kim, J.-H. Choi*, C.-H. Kim*, M.F. Chang and I. Verbauwhede, University of California, Los Angeles, CA, *Samsung Electronics, Hwasung, Korea*
- 11:45 am 3-5 A 10Gb/s Data-Dependent Jitter Equalizer,** *J. Buckwalter and A. Hajimiri, California Institute of Technology, Pasadena, CA*

Session 4 – Analog Filters
Grand Caribbean VI, Monday Morning, October 4

Chair: Takahiro Miki Co-Chair: Pat Rakers

Advanced analog filters are presented. Techniques for accurate tuning and low distortion are discussed. Filters for dual-mode transceiver and high bandwidth of 500 MHz are also demonstrated.

- 10:00 am Introduction**
- 10:05 am 4-1 A 0.8V Accurately-Tuned Continuous-Time Filter,** *G. Vemulapalli, P. K. Hanumolu, and U.-K. Moon, Oregon State University, Corvallis, OR*
- 10:30 am 4-2 A CMOS Gyrator Low-IF Filter for a Dual-Mode Bluetooth/ZigBee Transceiver,** *B. Guthrie, T. Sayers, A. Spencer, and J. Hughes, Philips Research Laboratories, Redhill, Surrey, England*
- 10:55 am 4-3 A 1.8V Triode-Type Transconductor and Its Application to a 10MHz 3rd-Order Chebyshev Low Pass Filter,** *Y.-H. Kim, J.-W. Park, M.-Y. Park, and H.-K. Yu, Electronics and Telecommunications Research Institute, Daejeon, Korea*
- 11:20 am 4-4 A 500 MHz OTA-C 4th Order Lowpass Filter with Class AB CMFB in 0.35 μ m CMOS Technology,** *P. Pandey, J. Silva-Martinez and X. Liu, Texas A&M University, College Station, TX*

Session 5 – Challenges and Trade-offs of SOC versus SIP
Grand Caribbean Ballroom VII, Monday Morning, October 4

Chair: Iraj Masarati Co-Chair: Rakesh Patel

This session explores SIP and SOC trade-offs for integration of memories, analog and RF. Also presented are an MRAM replacing flash in a SIP and a fully integrated GPS IC.

- 10:00 am Introduction**
- 10:05 am 5-1 Cellular Handset Integration -- SIP vs. SOC (INVITED),** *W. Krenik, D. Buss, and P. Rickert, Texas Instruments, Inc. Dallas, TX*

- 10:55 am** **MRAM and Microprocessor System-In-Package: Technology Stepping Stone to Advanced Embedded Devices (INVITED)**, *C.Trigas, S.Doll, and J.Kruecken, FreeScale Semiconductor, Munich, Germany*
- 5-2**
- 11:45 am** **23mm² Single-Chip 0.18µm CMOS GPS Receiver with 28mW-4.1 mm² Radio and CPU/DSP/RAM/ROM**, *G. Gramegna, M. Franciotta, V. Mandara, N.Bellantone, M.Vaiana, M.Paparo, M. Losi*, S. Das**, P.Mattos***, STMicroelectronics, Catania, Italy,, *STMicroelectronics, Agrate, Italy, **STMicroelectronics, Noida, India, ***STMicroelectronics, Bristol, United Kingdom*
- 5-3**

Session 6 – Specialized Custom Circuits
Boca Room II, Monday Morning, October 4

Chair: Jamil Kawa Co-Chair: Jackie Snyder

This session focuses on custom circuits that cover the spectrum of frequency hopping, power management, sizing for subthreshold operation, inductive cross talk management, and voltage doubling.

- 10:00 am** **Introduction**
- 10:05 am** **Observation of One-Fifth-of-a-Clock Wake-Up Time of Power-Gated Circuit**, *T.Miyazaki, T.Q. Canh, H. Kawaguchi and T. Sakurai, University of Tokyo, Tokyo, Japan*
- 6-1**
- 10:30 am** **Frequency-Hopping Vernier Clock Generators for Multiple Clock Domain SoCs**, *H. Kodama, M. Mizuno, K. Nose, and A. Tanaka, NEC Corp., Kanagawa, Japan*
- 6-2**
- 10:55 am** **Device Sizing for Minimum Energy Operation in Subthreshold Circuits**, *B. Calhoun, A. Wang and A. Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA*
- 6-3**
- 11:20 am** **Cross Talk Countermeasures in Inductive Inter-Chip Wireless Superconnect**, *N. Miura, D. Mizoguchi, T. Sakurai* and T. Kuroda, Keio University, Yokohama, Japan, *The University of Tokyo, Tokyo, Japan*
- 6-4**
- 11:45 am** **A Breakdown Voltage Doubler for High Voltage Swing Drivers**, *S. Mandegaran and A. Hajimiri, California Institute of Technology, Pasadena, CA*
- 6-5**

Session 7 – Simulation and Modeling for RF and Mixed Signal Designs
Grand Caribbean IV, Monday Afternoon, October 4

Chair: Steffen Rochel Co-Chair: Hidetoshi Onodera

This session presents automated macro modeling techniques for linear and non-linear circuits followed by advanced simulation techniques for RF designs.

- 2:00 pm** **Introduction**
- 2:05 pm** **An Overview of Automated Macromodelling Techniques for Mixed-Signal Systems (INVITED)**, *J. Roychowdhury, Univ. of Minnesota, Minneapolis, MN*
- 7-1**

- 2:55 pm **Automated Extraction of Broadly Applicable Nonlinear Analog Macromodels from SPICE-level Descriptions**, *N. Dong and J. Roychowdhury, University of Minnesota, Minneapolis, MN*
7-2
- 3:20 pm **Fast, Accurate Prediction of PLL Jitter Induced By Power-Grid Noise**, *X. Lai and J. Roychowdhury, University of Minnesota, Minneapolis, MN*
7-3
- 3:45 pm **Break**
- 4:00 pm **A Modified-Volterra-Series Technique for Improving the Accuracy of Quasi-Static Harmonic Balance Analysis in Coupled Device and Circuit Simulation**, *Y. Hu and K. Mayaram, Oregon State University, Corvallis, OR*
7-4
- 4:25 pm **An Efficient Algorithm for Simulating Error Vector Magnitude in Nonlinear OFDM Amplifiers**, *S. Yamanouchi, K. Kunihiro, and H. Hida, NEC Corporation, Ibaraki, Japan*
7-5
- 4:50 pm **Analysis of Envelope Signal Injection for Improvement of RF Amplifier Intermodulation Distortion**, *V. Leung, J. Deng, P. Gudem and L. Larson, University of California, San Diego, La Jolla, CA*
7-6

Session 8 – High-Performance Clocking and Digital Synthesis
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Grand Caribbean V, Monday Afternoon, October 4
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Chair: Cormac O'Connell Co-Chair: Johan van der Tang

This session showcases low jitter, wide range, DLL and PLL circuits for high-speed serial links. Also included are efficient direct digital frequency synthesizer architectures.

- 2:00 pm **Introduction**
- 2:05 pm **A 250MHz - 2GHz Wide Range Delay-Locked Loop**, *B.-G. Kim and L.-S. Kim, KAIST, Daejeon, Korea*
8-1
- 2:30 pm **A 2.5-3.125 Gb/s Quad Transceiver with Second Order Analog DLL Based CDRs**, *A. Coban, M. Koroglu and K. Ahmed, Mindspeed Technologies, Inc., Newport Beach, CA*
8-2
- 2:55 pm **A 2-5GHz Low Jitter 0.13µm CMOS PLL Using a Dynamic Current Matching Charge-Pump and a Noise Attenuating Loop-Filter**, *A. Maxim, Integrated Products, Austin, TX*
8-3
- 3:20 pm **An Improved CMOS Ring Oscillator PLL with Less than 4ps RMS Accumulated Jitter**, *S. Williams, H. Thompson, M. Hufford, and E. Naviasky, Cadence Design Services, Columbia, MD*
8-4
- 3:45 pm **Break**
- 4:00 pm **A 625 MHz to 10 GHz Clock Multiplier for ReTransmitting 10 Gb/s Serial Data**, *C.-W. Yao, H. Pham*, and A. Willson, Jr., University of California, Los Angeles, CA, *Promise Technology, Fremont, CA*
8-5

- 4:25 pm **A 1.5V Direct Digital Synthesizer with Tunable Delta**
8-6 **Sigma Modulator in 0.13 μ m CMOS**, J. Lindeberg, J. Vankka, J.Sommarek, and K. Halonen, Helsinki University of Technology, Espoo, Finland
- 4:50 pm **High-Speed Direct Digital Frequency Synthesizers in**
8-7 **0.25- μ m CMOS**, A. Strollo, D. De Caro, E. Napoli, and N. Petra, University of Naples, Italy

<p align="center">Session 9 – Precision Level Output Devices Grand Caribbean VI, Monday Afternoon, October 4</p>

Chair: David Rich Co-Chair: Rick Carley

This session presents new techniques to reduce errors in digital to analog converters. The second part of the session looks at data converters that produce 1-bit output streams for output drivers.

- 2:00 pm **Introduction**
- 2:05 pm **A 250 mW Class D Design with Direct Battery Hookup**
9-1 **in a 90 nm Process**, B. Forejt, V. Rentala, G. Burra, and J. Arteaga, Texas Instruments, Inc., Plano, TX
- 2:30 pm **A Class-D Amplifier Using a Spectrum Shaping**
9-2 **Technique**, A. Yasuda, T. Kimura*, K. Ochiai* and T. Hamasaki*, Hosei University, Tokyo, Japan, *Texas Instruments Japan, Inc., Kanagawa, Japan
- 2:55 pm **A Delta-Sigma Modulator for 1-Bit Digital Switching**
9-3 **Amplifier**, P. Lo Re, Y. Fujimoto, H. Tani and M. Miyamoto, Sharp Corporation, Nara, Japan
- 3:20 pm **Design of High-Performance Asynchronous Sigma**
9-4 **Delta Modulators with a Binary Quantizer with Hysteresis**, S. Ouzounov, E. Roza*, H. Hegt, G. van der Weide* and A. van Roermund, Eindhoven University of Technology, Eindhoven, The Netherlands, *Philips Research Laboratories, Eindhoven, The Netherlands
- 3:45 pm **Break**
- 4:00 pm **A Study Of Error Sources In Current Steering Digital-**
9-5 **to-Analog Converters (INVITED)**, D. Mercer, Analog Devices, Inc., Wilmington, MA
- 4:50 pm **GSM DAC with New Segmented Mismatch Shaping**
9-6 **Technique**, A. Shabra, J. Gealow and P. Ferguson, Jr., Analog Devices, Inc., Wilmington, MA

Session 10 – Design for Testability
Grand Caribbean VII, Monday Afternoon, October 4

Chair: Gordon Roberts Co-Chair: Robert Aitken

Enhancing the testability of a circuit design allows for improved product quality at reduced cost. This session includes novel techniques for high-speed I/Os, A/O converters, and Σ - Δ modulators.

- 2:00 pm Introduction**
- 2:05 pm Design Considerations and DFT to Enable Testing of Digital Interfaces (INVITED),** *M. Tripp, T. Mak and A. Meixner, Intel Corporation, Hillsboro, OR*
- 2:55 pm A Digital DFT Technique for Verifying the Static Performance of A/D Converters,** *W. Choi, B. Vinnakota and R. Harjani, University of Minnesota, Minneapolis, MN*
- 3:20 pm Design-for-Digital-Testability 30 MHz Second-Order Sigma-Delta Modulator,** *H.-C. Hong, National Chiao Tung University, Hsin-Chu, Taiwan*
- 3:45 pm Break**

Session 11 – CMOS Scaling and Alternatives
Boca Room II, Monday Afternoon, October 4

Chair: Larry Wissel Co-Chair: David Sunderland

This session covers conventional bulk CMOS scaling roadmap for both digital and RF applications, as well as alternative CMOS structures that could overcome roadblocks to scaling.

- 2:00 pm Introduction**
- 2:05 pm RFCMOS Technology from 0.25 μ m to 65nm: The State of the Art (INVITED),** *J. Pekarik, D. Greenberg, B. Jagannathan, R. Groves, J. Jones, R. Singh, A. Chinthakindi, X. Wang, M. Breitwisch, D. Coolbaugh, P. Cottrell, J. Florkey, G. Freeman and R. Krishnasamy, IBM SRDC, Essex Junction, VT*
- 2:55 pm Low Power Logic Circuit and SRAM Cell Applications with Silicon on Depletion Layer CMOS (SODEL CMOS) Technology,** *S. Inaba, H. Nagano, K. Miyano, I. Mizushima, Y. Okayama, T. Nakauchi, K. Ishimaru and H. Ishiuchi, Toshiba Corporation Semiconductor Company, Yokohama, Japan*
- 3:20 pm Opportunities and Challenges In Asymmetric Device Implementation,** *J. Buller, R. vanBentum**, J. Cheek*, E. Ehrichs, M. Horstmann**, S. Searles, AMD, Austin, TX, *AMD, East Fishkill, NY, **AMD, Dresden, Germany*
- 3:45 pm Break**
- 4:00 pm MOSFET Scaling Trends and Challenges Through the End of the Roadmap (INVITED),** *P. Zeitzoff, International SEMATECH, Austin, TX*

Session 12 – ESD Protection
Grand Caribbean VII, Monday Afternoon, October 5

Chair: Mike Zachariah Co-Chair: Rob Aitken

This session addresses a key element of IC reliability through presentation of silicon-proven approaches to 3D ESD circuit simulation, analysis of power networks and design window expansion.

- 3:55 pm Introduction**
- 4:00 pm A 3D Mixed-Mode ESD Protection Circuit Simulation-
12-1 Design Methodology, H. Xie, R. Zhan, H. Feng, G. Chen, A. Wang and R. Gafiteanu*, Illinois Institute of Technology, Chicago, IL, *Synopsys, Sunnyvale, CA**
- 4:25 pm Power Network Analysis for ESD Robustness in a
12-2 90nm ASIC Design System, C. Brennan, J. Kozhaya and R. Proctor, IBM Microelectronics Division, Essex Junction, VT**
- 4:50 pm Active-Source-Pump (ASP) Technique for ESD
12-3 Design Window Expansion and Ultra-Thin Gate Oxide Protection in Sub-90nm Technologies, M. Mergens, J. Armer*, P. Jozwiak*, B. Keppens, F. De Ranter, K. Verhaege, R. Kumar**, Sarnoff Europe, Gistel, Belgium, *Sarnoff Corporation, Princeton, NJ, **TCX, Inc., San Diego, CA**

Session 13 – Integrated Oscillators and Tuning Elements

Grand Caribbean IV, Tuesday Morning, October 5

Chair: Ranjit Gharpurey Co-Chair: Edoardo Charbon

The session begins with a discussion of MEMS for wireless applications. Two VCOs that achieve a wide tuning range by means of switched capacitor techniques are presented next. Finally, techniques for temperature desensitization and for inductor size optimization are proposed.

- 8:30 am Introduction**
- 8:35 am Vibrating RF MEMS for Next Generation Wireless
13-1 Applications (INVITED), C. Nguyen, University of Michigan, Ann Arbor, MI**
- 9:25 am A CMOS VCO with 48% Tuning Range for Modern
13-2 Broadband Systems, K. Manetakis, D. Jessie and C. Narathong, Qualcomm CDMA Technologies, San Diego, CA.**
- 9:50 am Break**
- 10:05 am 5-GHz In-Phase Coupled Oscillators with 39% Tuning
13-3 Range, L. Romano, V. Minerva, S. Cavalieri D'Oro*, C. Samori, and M. Politi, Politecnico di Milan, Milan, Italy, *Ericsson Lab Italy, Milan, Italy**

- 10:30 am** **A Temperature-Compensated CMOS LC-VCO**
13-4 **Enabling the Direct Modulation Architecture in**
2.4GHz GFSK Transmitter, T. Tanzawa, H. Shibayama,
R. Terauchi, K. Hisano, H. Ishikuro, S. Kousai, H.
Kobayashi, H. Majima, T. Takayama, K. Agawa, M.
Koizumi, and F. Hatori, Toshiba Corp., Kawasaki, Japan
- 10:55 am** **On the Selection of On-Chip Inductors for the**
13-5 **Optimal VCO Design, Y. Zhan, R. Harjani and S.**
Sapatnekar, University of Minnesota, Minneapolis, MN

<p>Session 14 – Custom Circuits for Interfaces and Imaging Grand Caribbean V, Tuesday Morning, October 5</p>
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Chair: Takayasu Sakurai Co-Chair: Tadahiro Kuroda

Circuit ideas for read channel, audio and image sensing applications are discussed with emphasis on high speed, low power or low noise considerations.

- 8:30 am** **Introduction**
- 8:35 am** **A 0.13 μ m CMOS Ultra-Compact DVD SoC Employing**
14-1 **a Full Digital Equalizing PRML Read Channel, K.**
Nagano, K. Okamoto, A. Yamamoto, H. Mouri, A.
Kawabe, H. Fujiyama, T. Morie, H. Nakahira, M.
Kuramochi, M. Ochiai, K. Aida, Y. Ogura, T. Takahashi,*
T. Kakiage, M. Takiguchi, T. Yamamoto, H. Kamiyama,
and Y. Katabe, Matsushita Electric Industrial Co., Ltd,
*Osaka, Japan, *Matsushita Kotobuki Ind., Ltd., Japan*
- 9:00 am** **An Improved Architecture of the Mixed Mode**
14-2 **Clock/Data Recovery for DVD Read Channel, J.E. Lee,**
H. Chae, H. Lee, M. Konakov, J.H. Lee and J.W. Lee,
SAIT, Suwon, Korea
- 9:25 am** **A 2W, 92% Efficiency and 0.01% THD+N Class-D**
14-3 **Audio Power Amplifier for Mobile Applications,**
Based on the Novel SCOM Architecture, S.-H. Lee, J.-
*Y. Shin, H.-Y. Lee, H.-J. Park, *K. Lund, *K. Nielsen, and*
J.-W. Kim, Samsung Electronics. Co., Gyeonggi-Do,
*Korea, *Bang & Olufsen ICEpower a/s, Lyngby, Denmark*
- 9:50 am** **Break**
- 10:05 am** **A Word-Parallel Digital Associative Engine with Wide**
14-4 **Search Range Based on Manhattan Distance, Y.**
Oike, M. Ikeda, and K. Asada, University of Tokyo,
Tokyo, Japan
- 10:30 am** **Multiple Integration Method for High Signal-to-Noise**
14-5 **Ratio Readout Integrated Circuit, S.G. Kang, D.H.**
Woo, and H.C. Lee, Korea Advanced Institute of Science
and Technology, Daejeon, Korea
- 10:55 am** **A 256-Element CMOS Imaging Receiver for Free-**
14-6 **Space Optical Communication, B. Leibowitz, B. Boser,**
K. Pister, University of California, Berkeley, CA

Session 15 – SOC Solutions for Nanometer Design
Grand Caribbean VI, Tuesday Morning, October 5

Chair: Ricki Dee Williams Co-Chair: Thomas Zimmermann

As SOC process technology scales, many problems ensue. This session starts with DFM, then discusses power management and different design techniques to provide insight into these problems and solutions.

8:30 am Introduction

**8:35 am Proactive Design For Manufacturing (DFM) for
15-1 Nanometer SoC Designs (INVITED), C. Guardiani, N. Dragone, P. McNamara, PDF Solutions, San Jose, CA**

**9:25 am Design and Development of 130-Nanometer ICs for a
15-2 Multi-Gigabit Switching Network System, A. Khan, K. Ruparel*, C. Joly*, V. Ghanta*, D. Le, T. Nguyen, J. Yu, S. Yang, I. Ahmed, N. Burnside, V. Chagarlamudi, M. Cheung, F. Chiu, Y. Fan, D. Ge, J. Gill, P. Huang, V. Jayapal, O. Kim, M. Li, H. Mak, P. McKeever, S. Nguyen, K. Rajan, S. Riley, P. Tran, H. Truong, A. Tsou, D. Wang, C. Yang, J. Zhang, and X. Zhong, Cadence Design Systems, San Jose, CA, *Cisco Systems, San Jose, CA**

9:50 am Break

**10:05 am An Electrically Robust Method for Placing Power
15-3 Gating Switches in Voltage Islands, J. Kozhaya and L. Bakir, IBM Microelectronics, Essex Junction, VT**

**10:30 am Differential Transmission Line Interconnect for High
15-4 Speed and Low Power Global Wiring, S. Gomi, K. Nakamura, H. Ito, K. Okada, K. Masu, Tokyo Institute of Technology, Yokohama, Japan**

**10:55 am A Soft-Error Hardened Latch Scheme for SoC in a
15-5 90nm Technology and Beyond, Y. Komatsu, Y. Arima, T. Fujimoto, T. Yamashita, and K. Ishibashi, Semiconductor Technology Academic Research Center, Yokohama, Japan**

**11:20 am Analog IP Migration Using Design Knowledge
15-6 Extraction, S. Hammouda, M. Dessouky*, M. Tawfik and W. Badawy**, Mentor Graphics Egypt, Cairo, Egypt, *Ain Shams University, Cairo, Egypt, **University of Calgary, Calgary, Alberta, Canada**

Session 16 – Advanced Memory Issues
Grand Caribbean VII, Tuesday Morning, October 5

Chair: Tom Andre Co-Chair: Jean-Christophe Vial

This session will present solutions to issues affecting advanced memories, including power reduction, speed improvement, process defect tolerance and soft error correction.

8:30 am Introduction

**8:35 am Reviews and Future Prospects of Low-Voltage
16-1 Embedded RAMs (INVITED), K. Itoh, K. Osada, and T. Kawahara, Hitachi, Ltd., Tokyo, Japan**

- 9:25 am 16-2** **BIST Controlled Variable Sense Amp Timing for 90nm Embedded SRAM**, C. Brennan, S. Eustis, J. Goss, A. Humphrey, M. Ouellette, J. Rowland, and M. Fragano, IBM Microelectronics Div., Essex Junction, VT
- 9:50 am** **Break**
- 10:05 am 16-3** **Design and Implementation of an Embedded 512KB Level 2 Cache Subsystem**, J.L. Shin, B. Petrick, H. Levy, J. Son, M. Singh, V. Mathur, J.-C. Yeh, H. Choi, V. Gupta, T. Ziaja and A. Leon, Sun Microsystems Inc., Sunnyvale, CA
- 10:30 am 16-4** **Process Variation in Nano-Scale Memories: Failure Analysis and Process Tolerant Architecture**, A. Agarwal, B. Paul, and K. Roy, Purdue University, West Lafayette, IN
- 10:55 am 16-5** **Analysis of SRAM Neutron-Induced Errors Based on the Consideration of Both Charge-Collection and Parasitic-Bipolar Failure Modes**, K. Osada, N. Kitai*, S. Kamohara**, T. Kawahara, Hitachi, Ltd., Tokyo, Japan, *Hitachi ULSI Systems Co., Ltd., Tokyo, Japan, **Renesas Technology Corp., Tokyo, Japan

<p>CICC Luncheon Grand Caribbean III, Tuesday, October 5 12:00 – 1:30 pm</p>

Impact of Nanoscale Science on Life Sciences and Medicine

Dr. Frederic Zenhausern
Director, Applied Nano-Bioscience Center, Arizona State University

When a patient is diagnosed with cancer, often large tissues are already affected. But these diseases started within a single cell. The “Nanoscale Life Science” projects at the Center for Applied Nanobioscience (ANBC) create integrated and miniaturized systems for robust and rapid nucleic acid diagnostic testing to enable the first pathological changes to be studied and diagnosed. The presentation reports on new devices for various applications including prototypes for pharmacogenomic diagnostics to predict patient responsiveness to cancer treatments, detect exposure to bioterror agents, and screen subjects for clinical trials. A first platform on melanoma treatment that performs hybridization-based bioassay 10x faster than conventional microarrays, and integrated platforms with on chip sample preparation are also described. ANBC will report its approaches for unconventional patterning technology of polymeric substrates to reach the sub-10 nm resolution required. Finally, the impact of miniaturization and integration of analog circuitry and sensors on flexible substrate for new low cost disposable platforms for biosensing are discussed.

Frederic Zenhausern attended the University of Geneva where he received a B.S. in Biochemistry and a Ph.D in Applied Physics in 1993. He received his MBA in Finance from Rutgers University in 2000. He joined IBM T. J. Watson Research Center in 1993 and then held several research positions at international corporate research laboratories, and more recently as Manager of Microdevice Physics (Motorola Labs). He has co-authored more than 40 scientific publications and thirteen U.S. patents.

Now, he’s Associate Professor and Director of the Center for Applied Nanobioscience (ANBC), a new venture between the College of Engineering

at Arizona State University and the AZBio Design Institute. He is also the R&D Director for the newly formed International Center for Flexible Displays, a cooperative agreement between the U.S. Army, universities and more than 20 industrial members. During the last 3 years, his team has successfully transferred integrated nano/micro-system technologies to product platforms.

Tickets for the Luncheon cost \$32 and can be purchased through Advance Registration. See the Registration form in the center of this Program.

Session 17 – RF Noise Modeling and Analysis

Grand Caribbean IV, Tuesday Afternoon, October 5

Chair: Yuhua Cheng Co-Chair: Hong-Ha Vuong

Join this session to get advanced research results on flicker and H.F. noise modeling and characterization, and on coupling analysis for RF components, circuits, and substrate.

- 2:00 pm Introduction**
- 2:05 pm 17-1 Analysis and Measurements of EM and Substrate Coupling Effects in Common RF Integrated Circuits,** *R. Amaya, P. Popplewell, M. Cloutier* and C. Plett*, Carleton University, Ottawa, Ont., Canada, *Skyworks Solutions, Inc., Ottawa, Ont., Canada*
- 2:30 pm 17-2 Digital Noise Coupling in a 2.4GHz LNA for Heavily and Lightly Doped CMOS Substrates,** *S. Hazenboom, T. Fiez and K. Mayaram, Oregon State University, Corvallis, OR*
- 2:55 pm 17-3 Crosstalk Coupling Effects of CMOS Co-Planar Spiral Inductors,** *J. Mikkelsen, O.K. Jensen and T. Larsen, Aalborg University, Aalborg, Denmark*
- 3:20 pm 17-4 Noise in Passive FET Mixers: A Simple Physical Model,** *S. Chehrazi, R. Bagheri, and A. Abidi, University of California, Los Angeles, CA*
- 3:45 pm Break**
- 4:00 pm 17-5 Analytical Modeling of MOSFET Noise Parameters for Analog and RF Applications,** *S. Asgaran, M. Deen and C.-H. Chen, McMaster Univ., Hamilton, Ont., Canada*
- 4:25 pm 17-6 Enhanced Analytic Noise Model for RF CMOS Design** *J. Koeppel and R. Harjani, University of Minnesota, Minneapolis, MN*
- 4:50 pm 17-7 Measurement and Modeling of Noise Parameters for Desensitized Low Noise Amplifiers,** *G. Banerjee, D. Becher, C. Hung, D. Allstot* and K. Soumyanath, Intel Corp., Hillsboro, OR, *Univ. of Washington, Seattle, WA*

**Session 18 – Single Chip Radio Solutions for
Wireless Communication**

Grand Caribbean V, Tuesday Afternoon, October 5

Chair: Oliver Werther Co-Chair: Stefan Drude

Fully integrated 1V Blue tooth transceiver, ultra low power 900 MHz transceiver, single chip implementations for wireless LAN applications and IF digitizing IC for EDGE/GSM base solutions are presented.

2:00 pm Introduction

**2:05 pm Design Techniques for a 1-V Operation Bluetooth RF
18-1 Transceiver (INVITED), M. Ugajin, A. Yamagishi, J. Kodate, M. Harada, and T. Tsukahara, NTT Microsystem Integrations Laboratories, Kanagawa, Japan**

**2:55 pm An Ultra-Low Power 900 MHz RF Transceiver for
18-2 Wireless Sensor Networks, A. Molnar, B. Lu, S. Lanzisera, B. Cook and K. Pister, University of California, Berkeley, CA**

**3:20 pm A Cost-Efficient 0.18 μ m CMOS RF Transceiver Using
18-3 a Fractional-N Synthesizer for 802.11b/g Wireless LAN Applications, N. Haralabidis, K. Vavelidis, I. Vassiliou, T. Georgantas, A. Yamanaka*, S. Kavadias, G. Kamoulakos, C. Kapnistis, Y. Kokolakis, A. Kyranas, P. Merakos, I. Bouras, S. Bouras and S. Plevridis, Athena Semiconductors S.A., Alimos, Greece, *Athena Semiconductors Inc., Fremont, CA**

3:45 pm Break

**4:00 pm A CMOS Direct-Conversion Transceiver for IEEE
18-4 802.11a/b/g WLANs, P. Zhang, L. Der, D. Guo, I. Sever, T. Bourdi, C. Lam, A. Zolfaghari, J. Chen, D. Gambetta, B. Cheng, S. Gower, S. Hart, L. Huynh, T. Nguyen and B. Razavi*, RF Micro Devices, San Jose, CA, *University of California, Los Angeles, CA**

**4:25 pm A Dual Channel IF-Digitizing IC with 117dB Dynamic
18-5 Range at 300MHz IF for EDGE/GSM Base-Stations, M. Hensley, C. Speir, R. Stop, K. Behel, C. Moreland, G. Patterson, D. Kelly*, M. Manglani, M. Elliott, S. Puckett, J. Young and F. Murden, Analog Devices, Inc., Greensboro, NC, *Analog Devices, Inc., Wilmington, MA**

Session 19 – Programmable Architectures

Grand Caribbean VI, Tuesday Afternoon, October 5

Chair: Steve Brown Co-Chair: John Wright

This session discusses technology advances for each major type of programmable device applicable to a wide range of digital system designs. Presentations include via-programmable, metal programmable, synthesizable cores, CPLDs, and the complex issue of I/O design for high-performance FPGAs.

2:00 pm Introduction

**2:05 pm Platform IC with Embedded Via Programmable Logic
19-1 for Fast Customization, L. Cali, F. Lertora, C. Gazzina, M. Besana and M. Borgatti, STMicroelectronics, Agrate Brianza, Italy**

- 2:30 pm 19-2** **Designing a Via-Configurable Regular Fabric**, *Y. Ran and M. Marek-Sadowska, University of California, Santa Barbara, CA*
- 2:55 pm 19-3** **Hybrid Approach to Structured ASICs for Minimizing the Impact of Reticule Costs and Interconnect Delay**, *J. Brown, R. Packer, J. Prasad, K. Kofford, T. Dye, and B. Kirk, AMI Semiconductor, Inc., Pocatello, ID*
- 3:20 pm 19-4** **A 90nm FPGA I/O Buffer Design with 1.6Gbps Data Rate for Source-Synchronous System and 300MHz Clock Rate for External Memory Interface**, *J. Tyhach, B. Wang, C. Sung, J. Huang, K. Nguyen, X. Wang, Y. Chong, P. Pan, H. Kim, G. Rangan, T-C.. Chang, J. Tan, Altera Corporation, San Jose, CA*
- 3:45 pm** **Break**
- 4:00 pm 19-5** **Sequential Synthesizable Embedded Programmable Logic Cores for System-on-Chip**, *A. Yan and S. Wilton, University of British Columbia, Vancouver, B.C., Canada*
- 4:25 pm 19-6** **A High Performance CMOS Programmable Logic Core**, *Y. Han, L. McMurchie and C. Sechen, University of Washington, Seattle, WA*
- 4:50 pm 19-7** **MAX II: A Low-Cost, High-Performance LUT-Based CPLD**, *P. Leventis, B. Vest*, M. Hutton*, D. Lewis, Altera Corporation, Toronto, Ont., Canada, *Altera Corporation, San Jose, CA*

Session 20 – Memory Trends

Grand Caribbean VII, Tuesday Afternoon, October 5

Chair: Betty Prince Co-Chair: Takashi Akioka

This session presents trends in memories including challenges in embedded and emerging memory, future embedded DRAM using single electron concepts, advanced ternary CAM and anti-fuse.

- 2:00 pm** **Introduction**
- 2:05 pm 20-1** **Trends and Challenges of Large Scale Embedded Memories (INVITED)**, *T. Furuyama, Toshiba Corporation, Kawasaki, Japan*
- 2:55 pm 20-2** **SESO Memory: A 3T Gain Cell Solution Using Ultra Thin Silicon Film for Dense and Low Power Embedded Memories (INVITED)**, *T. Ishii, T. Osabe, T. Mine, T. Sano*, B. Atwood, N. Kameshiro, T. Watanabe and K. Yano, Hitachi, Ltd., Tokyo, Japan, *Renesas Northern Japan Semiconductor Inc.*
- 3:45 pm** **Break**
- 4:00 pm 20-3** **Advanced Ternary CAM Circuits on 0.13 μ m Logic Process Technology**, *A. Roth, D. Foss, R. McKenzie, D. Perry, MOSAID Technologies, Kanata, Ont., Canada*
- 4:25 pm 20-4** **Pure CMOS One-Time Programmable Memory Using Gate-Ox Anti-Fuse**, *H. Ito and T. Namekawa, Toshiba Corporation, Kawasaki, Japan*

Session 21 – Evening Panel Discussion
Grand Caribbean Ballroom IV, Tuesday, October 5, 8:00 pm

MEMS and Nanotechnology - Hot or Hype?

Organizers: Mike Beunder, Cavendish Kinetics

Moderator: Jeanne Trinko Mechler, IBM

Panelists:

Michael Despont, IBM Research

Ron Dizy, Celtic House Venture Partners

Paul Hedges, Cavendish Kinetics

Kris Baert, IMEC

Dan Hyman, Xcom Wireless

Bill Price, Philips Semiconductors

Paul McWhor, Sandia Laboratories

Micro-electromechanical systems, or MEMS, and nanotechnology have been billed as "The Next Big Thing" by many industry analysts. Technology companies and government laboratories have been pouring billions of dollars into research and development into the design and manufacturing processes which allow tiny mechanical devices such as sensors for temperature, pressure, and vibration, valves, actuators, micro mirrors, gyroscopes, and other micro-scale mechanical devices to be embedded into semiconductor chips. Commercial applications for MEMS range from automotive where MEMS sensors are used for pressure and acceleration measurement or airbag deployment, to optical telecommunications RF switches, to construction where building materials sense changes in mechanical stresses and medical applications where MEMS are used in micron-sized blood pressure sensors, disposable angioplasty devices which monitor pressure in balloon catheters, kidney dialysis pressure sensors or airflow sensors in respiratory equipment. But is the price tag too high for MEMS development and manufacturing, which has been estimated by Vertical Market Research at \$3.3 billion US R&D dollars by 2007, and will the payback be too little too late?

The recent technology slump saw a number of MEMS design and manufacturing companies go under, including OnStream MST which made wireless MEMS switches, Optical Micro Machines (OMM), Transparent Networks, and Standard MEMS. MEMSCAP, with 256 employees worldwide, which bills itself as the first and only publicly listed purely MEMS company in the world, has had back to back fiscal losses putting its future in question. On the other hand, major corporations such as IBM, Intel, AMD, Siemens, Phillips, Hitachi, TSMC, NEC, UMC, Toshiba and others are making key advances and key investments in the field. Small Times News cites other companies who have been successful in the nanotechnology arena such as BEI Technologies Inc in automotive and military MEMS gyros and sensors, Form Factor Inc with dense wafer probe cards, NanoOpto Corp with nano-imprinting for telecommunications and ObducatAB with their Nanoprint Lithography. Does this tell us that MEMS fit only into niche applications and markets and only companies with deep pockets can afford to solve the MEMS manufacturing challenges with specialized processes? Will MEMS become ubiquitous on semiconductor chips or remain in the specialty application space? Where are the newest MEMS applications which will drive them into mainstream foundries? If MEMS and nanotechnology are the Next Big Thing, WHEN will they reach that status and start to pay dividends against the R&D investments?

Session 22 – Evening Panel Discussion
Grand Caribbean Ballroom V, Tuesday, October 5, 8:00 pm

Are ASICs Dying Because of FPGAs and the Price of Software?

Organizer/Moderator: Stephen Brown, Altera

Panelists:

Antun Domic, Senior V.P.,
Synopsys

Ken McElvain, CEO, Synplicity

Hugh Durdan, V.P. Altera

Steve Sutton, V.P., Texas
Instruments (ASICs)

Vince Hopkin, V.P., AMI
Semiconductor

Stephen Trimberger,
Distinguished Engineer, Xilinx

This panel session asks two intertwined questions--first, "Are ASICs dying?" Our panel members will interpret the relevant facts, probably with some disagreement. There are those who may site a reduced number of ASIC design starts, while others may point to a stability of the ASIC market share as a percentage of the global CMOS logic market. Some interesting issues to explore include: How many ASIC design starts happened last year, and are forecasted for next? What are the competitive pressures against ASICs? Which technology nodes are seeing the most action, and why? What are the motivations for using the latest technology? What are the challenges of 65nm and beyond, for both ASICs and FPGAs? These complex issues should make for an interesting discussion.

The second question looks at the effect on ASICs of competition from FPGAs, and the implications of CAD software prices. Our expert panel members will examine the market forces that determine which technology is chosen for each newly-developed digital product: What are the foundry costs for manufacturing a new chip? How many logic gates are needed for modern applications? What system speed is required? What is the volume of chip sales that can be expected? What are the various components of a typical development schedule and how much do contribute to the total cost? What is the life expectancy of a product? What software features are needed? What is the return on investment?

This panel features two experts in the areas of standard cell ASICs and structured ASICs, two experts on FPGA technology, and two experts on CAD software for both ASICs and FPGAs. This list of advocates should make for a dynamic and exciting discussion.

Session 23 – Evening Panel Discussion
Grand Caribbean Ballroom VI, Tuesday, October 5, 8:00 pm

SOC vs. SIP; Are We Putting Too Much On One Chip?

Organizers: Robert Aitken, Artisan Components

Moderator: Lawrence Clark, University of New Mexico

Panelists:

Pieter Hooijmans, Philips

Kenneth Brown, Intel

Anthony Gadlent, Cadence

Peter Rickert, Texas
Instruments

David Allstot, University of
Washington

With every generation, CMOS scaling makes additional chip area available to designers. For several generations now, designers have taken advantage of this extra area by integrating functions that were previously on multiple chips into a single die, a so-called System-on-Chip (SoC). Initially, SoC integration was primarily limited to digital circuitry, embedded SRAM, and processor cores. Recently, advances in technology have made possible the integration of other circuitry, including analog and mixed signal, DRAM, flash and even RF.

However, just because something is feasible does not necessarily make it desirable. The panel addresses the question of whether we have pushed the bounds of integration too far -- should we build a single chip radio or embedded flash, or are other approaches, such as System-In-Package, better? The panelists have broad experience in the field and will address the question from both technological and business standpoints.

Session 24 – Interconnect and Noise Modeling
Grand Caribbean IV, Wednesday Morning, October 6

Chair: Elliot Gould Co-Chair: Albert Stritter

This session discusses inductance and capacitance extraction methods, interconnect modeling, noise coupling, and dynamic power integrity analysis.

8:30 am Introduction

8:35 am Relative Inductance Extraction Method, *K. Shakeri and J. Meindl, Georgia Institute of Technology, Atlanta, GA*

9:00 am Efficient Capacitance Extraction Method for Interconnects with Dummy Fills, *A. Kurokawa, T. Kanamoto*, A. Kasebe**, Y. Inoue***, and H. Masuda, Semiconductor Technology Academic Research Center, Kanagawa, Japan, *Renesas Technology Corp., Hyogo, Japan, **Meitec Corp., Tokyo, Japan, ***Waseda University, Kitakyushu, Japan*

9:25 am Performance Limitation of On-chip Global Interconnects for High-Speed Signaling, *A. Tsuchiya, Y. Gotoh, M. Hashimoto, and H. Onodera, Kyoto University, Kyoto, Japan, *PRESTO, JST., Japan*

9:50 am Break

- 10:05 am 24-4** **EPEEC: A Compact Reluctance Based Interconnect Model Considering Lossy Substrate Eddy Currents**, *R. Jiang and C.C.-P. Chen**, *University of Wisconsin, Madison, WI*, **National Taiwan University, Taipei, Taiwan*
- 10:55 am 24-5** **A Surface Potential Model for Predicting Substrate Noise Coupling in Integrated Circuits**, *S. Kristiansson, F. Ingvarson, S. Kagganti, and K. Jeppson*, *Chalmers University of Technology, Gothenburg, Sweden*
- 11:20 am 24-6** **Impact of Technology Scaling on Substrate Noise Generation Mechanisms**, *M. Badaroglu, P. Wambacq, G. Van der Plas, S. Donnay, G. Gielen**, and *H. De Man*, *IMEC, Leuven, Belgium*, **ESAT, K.U. Leuven, Belgium*
- 11:45 am 24-7** **Analysis of Coupling Noise and It's Scalability in Dynamic Circuits**, *M. Chowdhury and Y. Ismail*, *Northwestern University, Evanston, IL*
- 12:10 pm 24-8** **Full-Chip Vectorless Dynamic Power Integrity Analysis and Verification Against 100uV/100ps-Resolution Measurement**, *S. Lin, M. Nagata**, *K. Shimazaki***, *K. Satoh***, *M. Sumita***, *H. Tsujikawa*** and *A. T. Yang*, *Apache Design Solutions, Inc., Mountain View, CA*, **Kobe University, Kobe, Japan*, ***Matsushita Electric Industrial Co., Ltd., Nagaokakyo, Japan*

<p align="center">Session 25 – Oversampled Analog-to-Digital Converters Grand Caribbean V, Wednesday Morning, October 6</p>
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Chair: Don Thelen Co-Chair: Doug Garrity

This session is comprised of papers that describe low-power and multi-bit techniques for the development of oversampled analog-to-digital converters for lowpass applications.

- 8:30 am** **Introduction**
- 8:35 am 25-1** **A 1.2-V 15-bit 2.5-MS/s Oversampling ADC with Reduced Integrator Swings**, *K. Nam, S.-M. Lee, D. Su and B. Wooley*, *Stanford University, Stanford, CA*
- 9:00 am 25-2** **A Low-Voltage Low-Power Sigma-Delta Modulator with Improved Performance in Overload Condition**, *H. Thompson, M. Hufford, W. Evans, E. Naviasky*, *Cadence Design Services, Columbia, MD*
- 9:25 am 25-3** **Experimental Verification of a Correlation-Based Correction Algorithm for Multi-Bit Delta-Sigma ADCs**, *X. Wang, Y. Guo, U-K. Moon and G. Temes*, *Oregon State University, Corvallis, OR*
- 9:50 am** **Break**
- 10:05 am 25-4** **Linearity Enhancement Techniques in Low OSR, High Clock Rate Multi-Bit Continuous-Time Sigma-Delta Modulators**, *S. Paton**, *T. Potscher*, *A. Di Giandomenico*, *K. Kolhaupt*, *L. Hernandez**, *A. Wiesbauer*, *M. Clara*, and *R. Frutos**, *Infineon Technologies, Villach, Austria*, **Universidad Carlos III, Madrid, Spain*

10:30 am 25-5 Efficient Sampling of Reference Noise in a Switched Capacitor Sigma Delta ADC, I. O'Connell and C. Lyden*, National University of Ireland, Cork, Ireland, *Analog Devices, Cork, Ireland

10:55 am 25-6 A Sigma-Delta ADC with a Built-in Anti-Aliasing Filter for Bluetooth Receiver in 130nm Digital Process, J. Koh, K. Muhammad, B. Staszewski, G. Gomez and B. Horoun, Texas Instruments, Inc., Dallas, TX

Session 26 – Wireless Transmitters
Grand Caribbean VI, Wednesday Morning, October 6

Chair: Ali Niknejad Co-Chair: Earl McCune

The session begins with an invited talk presenting SOI technology for RF applications. Subsequent papers present new methods for transmitter design, including polar and digital modulation techniques.

8:30 am Introduction

8:35 am 26-1 Design and Manufacturability Aspect of SOI CMOS RFICs (INVITED), J. Kim, J.-O. Plouchart and N. Zamdmer, IBM SRDC, Hopewell Junction, NY

9:25 am 26-2 An All-Digital Universal RF Transmitter, P. Wagh, P. Midya, P. Rakers, J. Caldwell and T. Schooler, Motorola Laboratories, Schaumburg, IL

9:50 am Break

10:05 am 26-3 A 5-GHz Silicon Bipolar Transmitter Front-End for Wireless LAN Applications, A. Italia, L. La Paglia*, A. Scuderi*, F. Carrara, E. Ragonese, and G. Palmisano, Universita di Catania, Catania, Italy, *STMicroelectronics, Catania, Italy

10:30 am 26-4 A CMOS High Efficiency +22dBm Linear Power Amplifier, Y. Ding and R. Harjani*, Bernai Inc, Minnetonka, MN, *Univ. of Minnesota, Minneapolis, MN

10:55 am 26-5 A 24GHz, +14.5dBm Fully-Integrated Power Amplifier in 0.18 μ m CMOS, A. Komijani and A. Hajimiri, California Institute of Technology, Pasadena, CA

11:20 am 26-6 A Highly Integrated Quad Band Low Evm Polar Modulation Transmitter For GSM/EDGE Applications, A. Hadjichristos, J. Walukas, N. Klemmer, W. Suter, S. Justice, S. Uppathil, G. Scott, Ericsson Mobile Platforms, Research Triangle Park, NC

11:45 am 26-7 High Performance Open-Loop AM Modulator Designed for Power Control of E-GPRS Polar Modulated Power Amplifier, D. R. Pehlke, A. Hadjichristos, and S. Justice, Ericsson Mobile Platforms, Research Triangle Park, NC

Session 27 – Signal and Data Processors
Grand Caribbean VII, Wednesday Morning, October 6

Chair: Lawrence Clark Co-Chair: Ram Krishnamurthy

This session presents recent advances in integrated circuits employing programmable and reconfigurable architectures for low power, high performance communications and multimedia signal processing applications.

8:30 am Introduction

8:35 am Sandblaster Low Power DSP (INVITED), J. Glossner, K. Chirca, M. Schulte, H. Wang, N. Nasimzada, D. Har, S. Wang, A. Hoane, Jr., G. Nacer, M. Moudgill and S. Vassiliadis*, Sandbridge Technologies, White Plains, NY, *Delft University of Technology, Delft, The Netherlands,

9:25 am A 4.75GOPS Single-Chip Programmable Processor Array Consisting of a Multithreaded Processor and Multiple SIMD and IO Processors, Y.-D. Bae and I.-C. Park, KAIST Daejeon, Republic of Korea

9:50 am Break

10:05 am A Baseband Processor For Pulsed Ultra-Wideband Signals, R. Blazquez, P. Newaskar, F. Lee, and A. Chandrakasan, Mass. Inst. of Tech., Cambridge, MA

10:30 am The Performance and Experimental Results of a Multiple Bit Rate Symbol Timing Recovery Circuit for PSK Receivers, M. Yuce, W. Liu*, B. Bharat, J. Damiano, and P. Franzon, North Carolina State Univ., Raleigh, NC, *Univ. of California, Santa Cruz, CA

10:55 am A XiRisc-Based SoC for Embedded DSP Applications, M. Bocchi, C. De Bartolomeis, C. Mucci, F. Campi, A. Lodi, M. Toma, R. Canegallo* and R. Guerrieri, University of Bologna, Bologna, Italy, *STMicroelectronics, Agrate Brianza, Italy

11:20 am An Image Recognition Processor Using Dynamically Reconfigurable ALU, N. Miyamoto, K. Kotani, K. Maruo* and T. Ohmi, Tohoku University, Sendai, Japan, *Advantest Laboratories, Ltd., Sendai, Japan

Session 28 – Broadband Circuits and Frequency Synthesis

Grand Caribbean IV, Wednesday Afternoon, October 6

Chair: Francesco Svelto Co-Chair: Peter Kinget

Techniques for broad-band circuit design are proposed. Applications include an LNA for ultra-wide band, a DC-10GHz attenuator, a Ku-band tuner for satellite applications and a 21-27GHz power combiner. The session further discusses two fast locking frequency synthesizers and a technique for improved frequency ratio measurements.

1:30 pm Introduction

1:35 pm A Broadband Low-Noise Front-End Amplifier for Ultra Wideband in 0.13 μ m CMOS, R. Gharpurey, University of Michigan, Ann Arbor, MI

- 2:00 pm** **A DC-10GHz Linear-in-dB Attenuator in 0.13 μ m**
28-2 **CMOS Technology**, *H. Dogan, R. Meyer, A. Niknejad,*
University of California, Berkeley, CA
- 2:25 pm** **A Ku-Band Monolithic Tuner-LNB for Satellite**
28-3 **Applications**, *G. Giraldo, T. Copani*, S. Smerzi, and G.*
Palmisano, STMicroelectronics, Catania, Italy,*
**University of Catania, Catania, Italy*
- 2:50 pm** **A 21-27GHz Self-Shielded 4-Way Power-Combining**
28-4 **PA Balun**, *T.S.D. Cheung, J. Long*, Y. Tretiakov**, D.*
*Haramé**, University of Toronto, Toronto, Ont., Canada,*
**Delft University of Technology, Delft, The Netherlands,*
***IBM Microelectronics, Burlington, VT.*
- 3:15 pm** **Break**
- 3:30 pm** **Improved Method for Measuring Frequency Ratios in**
28-5 **GSM Mobile Phones**, *P. Bode, A. Lampe, M.*
Helfenstein, and M. Gollnick**, Philips Semiconductors,*
*Nuremberg, Germany, *Philips Semiconductors Zurich,*
*Switzerland, **Fachhochschule Brandenburg, Germany*
- 3:55 pm** **8GHz, 20mW, Fast Locking, Fractional-N Frequency**
28-6 **Synthesizer with Optimized 3rd Order, 3/5-Bit IIR and**
3rd Order 3-b FIR Noise Shapers in 90nm CMOS, *A.*
Ravi, R. Bishop, L. Carley, K. Soumyanath, Intel Corp.,*
*Hillsboro, OR, *Carnegie Mellon Univ., Pittsburgh, PA*
- 4:20 pm** **A 3.5GHz Integer-N PLL with Dual On-Chip Loop**
28-7 **Filters and VCO Tune Ports For Fast Low-IF/Zero-IF**
LO Switching In an 802.11 Transceiver, *S. Gierkink, D.*
Li, R. Frye** and V. Boccuzzi, Agere Systems,*
*Allentown, PA, *Intel, San Diego, CA, **RF Design*
Consulting, Piscataway, NJ

<p>Session 29 – Analog Techniques Grand Caribbean V, Wednesday Afternoon, October 4</p>

Chair: David Naim Co-Chair: David Allee

Analog circuits rely on low-voltage references, good component matching and often trimming circuits. Furthermore high-speed operation frequently relies on advanced processes and innovative circuits.

- 1:30 pm** **Introduction**
- 1:35 pm** **Design Considerations of Recent Advanced Low-**
29-1 **Voltage Low-Temperature-Coefficient CMOS Band-**
gap Voltage Reference (INVITED), *P.K.T. Mok and K.N.*
Leung, The Hong Kong University of Science and
Technology, Clear Water Bay, Hong Kong
- 2:25 pm** **Optimum Area Allocation for Minimum Mismatch**, *B.*
29-2 *Gregoire, AMI Semiconductor, Bozeman, MT*
- 2:50 pm** **A Programmable Floating-Gate Voltage Reference in**
29-3 **0.5 μ m CMOS**, *S. Cook, K. Layton, W. Marble, D. T.*
Comer, D. J. Comer*, C. Petrie*, AMI Semiconductor,*
*American Fork, UT, *Brigham Young Univ., Provo, UT*
- 3:15 pm** **Break**

- 3:30 pm** **A 531nW/MHz, 128x32 Current-Mode Programmable**
29-4 **Analog Vector-Matrix Multiplier with Over Two**
 Decades of Linearity, *R. Chawla, A. Bandyopadhyay, V.*
 Srinivasan and P. Hasler, Georgia Institute of
 Technology, Atlanta, GA
- 3:55 pm** **An 8bit 3GHz Si/SiGe HBT Sample-and-Hold**, *J.*
29-5 *Jensen and L. Larson**, *Intel Corp., San Diego, CA,*
 **University of California, San Diego, CA*
- 4:20 pm** **Variable Gain Differential Current Feedback**
29-6 **Amplifier**, *I. Koudar, AMI Semiconductor, Brno, Czech*
 Republic

Session 30 – Introduction to Silicon Debug and SOC Test

Grand Caribbean VI, Wednesday Afternoon, October 6

Chair: Rob Aitken Co-Chair: Gordon Roberts

This invited session includes tutorial-style presentations on the challenges of silicon debug and one company's approach to implementing a proposed IEEE standard on modular SOC test.

- 1:30 pm** **Introduction**
- 1:35 pm** **The Crazy Mixed Up World of Silicon Debug**
30-1 **(INVITED)**, *D. Josephson and B. Gottlieb** , *Hewlett-*
 *Packard Company, Fort Collins, CO, *Intel Corporation,*
 Santa Clara, CA,
- 2:25 pm** **Infrastructure for Modular SOC Testing (INVITED)**, *E.*
30-2 *Marinissen, T. Waayers, Philips Research Laboratories,*
 Eindhoven, The Netherlands
- 3:15 pm** **Break**

Session 31 – Emerging Techniques in SIP and SOC

Grand Caribbean VII, Wednesday Afternoon, October 6

Chair: Jose Cruz-Albrecht Co-Chair: Rich Liu

This session presents the latest innovations in technologies integrating systems in packages and on chips including MEMS, antennae, thin-film inductors and sensors.

- 1:30 pm** **Introduction**
- 1:35 pm** **System In Package - "The Rebirth of SIP" (INVITED)**,
31-1 *K. Brown, Intel Corporation, Chandler, AZ*
- 2:00 pm** **Factors Influencing the Design of Microsystems**
31-2 **(INVITED)**, *L. Spangler, Aspen Technologies, Colorado*
 Springs, CO
- 2:25 pm** **Low-Noise CMOS Integrated Sensing Electronics for**
31-3 **Capacitive MEMS Strain Sensors**, *M. Suster, J. Guo,*
 N. Chaimanonart, W.H. Ko, and D. Young, Case Western
 Reserve University, Cleveland, OH
- 2:50 pm** **10x Improvement of Power Transmission over Free**
31-4 **Space Using Integrated Antennas on Silicon**
 Substrates, *J.-J. Lin, X. Guo, R. Li, J. Branch, J. Brewer,*
 and K. K. O, University of Florida, Gainesville, FL

3:15 pm Break

3:30 pm 31-5 A 328 μ W 5 GHz Voltage-Controlled Oscillator in 90 nm CMOS with High-Quality Thin-Film Post-Processed Inductor, *D. Linten, X. Sun, G. Carchon, W. Jeamsaksiri, A. Mercha, J. Ramos, S. Jenei, L. Aspemyr*, A. Scholten**, P. Wambacq, S. Decoutere, S. Donnay, and W. De Raedt, Inter-University Micro-Electronics Center (IMEC), Leuven, Belgium, *Ericsson AB, Molndal, Sweden, **Philips Research, Eindhoven, The Netherlands*

3:55 pm 31-6 A CMOS 3D Camera with Millimetric Depth Resolution, *C. Niclass, A. Rochas, P. Besse, and E. Charbon, Swiss Federal Institute of Technology, Lausanne, Switzerland*

<p>Session 32 – Low Power Issues for FPGAs Grand Caribbean VI, Wednesday Afternoon, October 6</p>
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Chair: Steve Wilton Co-Chair: Brian Fitzgerald

Power issues have emerged as a key concern for the design of modern FPGAs, especially in 90 nm and beyond. This session discusses these concerns and provides some suggestions for solutions.

3:25 pm Introduction

3:30 pm 32-1 Power Estimation and Thermal Budgeting Methodology for FPGAs, *H. Lui, C. Lee and R. Patel, Altera Corporation, San Jose, CA*

3:55 pm 32-2 Low Leakage Circuit Design for FPGAs, *L. Ciccarelli, A. Lodi and R. Canegallo*, University of Bologna, Bologna, Italy, *STMicroelectronics, Agrate Brianza, Italy*

4:20 pm 32-3 A Novel Low-Power FPGA Routing Switch, *J. Anderson and F. Najm, University of Toronto, Toronto, Ontario, Canada*

GENERAL INFORMATION

LOCATION Caribe Royale Resort Suites
8101 World Center Drive
Orlando, FL 32821
(407) 238-8000
www.cariberoyale.com

REGISTRATION

Payment of the Technical Session registration fee entitles the registrant to entrance to all Monday-Wednesday, Technical Sessions, the Exhibit Hall, Exhibitor Preview Sessions, Exhibitor's Reception, Tuesday Happy Hour and one copy of the Conference Proceedings. Single-day registration entitles the registrant to that day's events and one copy of the Conference Proceedings. Technical session registration does not include entrance to the Sunday Educational Sessions.

Payment of the Sunday Educational Sessions registration fee entitles the registrant to entrance to the Sunday Educational Sessions, lunch on Sunday, and one copy of the Educational Sessions Workbook. Educational Session registration does not include entrance to the Monday-Wednesday Technical Sessions, the Exhibits or a copy of the Conference Proceedings.

To register online for the Technical Sessions and/or Sunday Educational Sessions go to the CICC website at www.ieee-cicc.org. Click on Registration.

To register by fax or mail fill out the registration form in the center of this booklet and fax or mail the form and payment to be received by **September 17**.

Don't register online and by mail or fax –it will result in double billing!

Online and mail/fax registration forms MUST be received by Friday, September 17

After that date please register onsite at the conference.

Make checks payable to CICC 2004 in US dollars on a US bank. We also accept **VISA** and **MasterCard only**. CICC is not able to accept American Express charges. Requests for cancellations must be received by September 17, 2004 to qualify for a refund.

The Registration Center, located in the Grand Caribbean Foyer, will be open as follows:

Registration for Sunday Educational Sessions Only

Sunday, Oct. 3 7:00 am - 2:00 pm

Registration for Technical Sessions

Sunday, Oct. 3 2:00 pm - 5:00 pm

Monday, Oct. 4 7:30 am - 5:00 pm

Tuesday, Oct. 5 8:00 am - 5:00 pm

Wednesday, Oct. 6 8:00 am - 3:00 pm

HOTEL ACCOMMODATIONS

The Caribe Royale Resort Suites is located at 8101 World Center Drive, Orlando, FL. The Caribe Royale is an "all suites" hotel. Every room has a bedroom and a living/dining room. Parking at the Hotel is free. The hotel is only 1.5 miles from the Walt Disney World Resorts®, features five restaurants and includes an outdoor swimming pool with a waterslide and a hot tub.

Room rates are \$169/Queen double room, \$179/Standard King, \$189/King Deluxe, \$294/Executive Suite, \$294/Villa. All rooms must be guaranteed with a credit card. To make a hotel reservation call the hotel at (407) 238-8000 or go to the CICC website www.ieee-cicc.org, click

on the General Information button on the left side of the page. Click on Hotel Reservations, then complete the form. The password is IEEE.

The hotel reservation cut-off date is Thursday, September 2. Please make your hotel reservations by this date in order to qualify for the CICC discount. Reservations made after September 2 will be on a space available and rate available basis.

You will receive a reservation confirmation directly from the hotel. It is the responsibility of each participant to make changes or cancellations directly with the hotel no later than 72 hours prior to scheduled arrival. No refunds will be given by the hotel for changes or cancellations with less than 72 hours notification.

EDUCATIONAL SESSIONS

On Sunday, Oct. 3, the CICC sponsors three Educational Sessions.

These Sessions are:

1. Advanced RF: From Devices to Systems
2. Advanced Data Converter Design Techniques
3. High-Performance and Low-Power Microprocessor Design Strategies

To register, complete the Advance Registration Form.

EXHIBITORS' RECEPTION

Monday Evening, Oct. 4, 5:30 pm - 7:00 pm
Grand Caribbean I/II Ballroom

The CICC social event this year is an Exhibitors' Reception sponsored by the CICC 2004 and IBM Microelectronics, held in the Exhibit Hall. All conference attendees are cordially invited! Enjoy the evening by browsing around the exhibit area, talking with the exhibitors' staff, seeing old friends and meeting new ones. Join us at the Exhibitors' Reception to celebrate this year's conference.

CICC LUNCHEON

The CICC Luncheon features an address titled "Impact of Nanoscale Science on Life Sciences and Medicine", by Dr. Frederic Zenhausern, Director, Applied Nano-Bioscience Center, Arizona State University. The luncheon is Tuesday, October 5, 12:00 noon – 1:30 pm. Luncheon is not included in the registration fee. Luncheon tickets are available through Advance Registration or onsite at a cost of \$32 per ticket for conference attendees only. See page 19 for a description of the presentation.

HAPPY HOUR

Tuesday Evening, October 5, 5:30 pm – 7:00 pm
Grand Caribbean I/II Ballroom

After a long day at the conference, the Tuesday Happy Hour is welcome break before the Panel Discussions. Tuesday night is the last night the Exhibit Hall is open so join us for a final visit with the exhibitors.

EVENING PANEL DISCUSSIONS

On Tuesday evening, Oct. 5, beginning at 8:00 pm, the CICC will offer three evening panel discussions on timely issues:

1. MEMS and Nanotechnology – Hot or Hype?
2. Are ASICs dying because of FPGAs and the price of software?
3. SOC vs. SIP; Are we putting too much on one chip?

CONFERENCE PROCEEDINGS

The proceedings contains papers on each presentation. Technical Session registrants will receive one copy of the Proceedings. Additional copies will be available at the conference registration desk, IEEE member: \$80, Non-member: \$90. After the conference, order the Proceedings through: Single Copy Sales, IEEE Service Center, 445 Hoes Lane, Box 1331, Piscataway, NJ, 08855-1331, Customer Service Department (toll free): 800-678-4333. The IEEE catalogue number is 04CH37571.

Approximately 6 weeks after the conference, technical session registrants will be mailed the conference CD ROM which includes copies of the papers and presentation slides. CICC gratefully acknowledges Philips Semiconductors' sponsorship of this CD ROM.

AUTHOR INTERVIEWS

There will be author interviews each day of the conference immediately following the afternoon sessions in Grand Caribbean Ballroom III. This additional forum provides an opportunity for relaxed discussions with your colleagues outside the strict time constraints of the regular sessions.

SPONSOR EVENTS

CICC acknowledges the generous support of our conference sponsors

- Philips Semiconductors for the Proceedings CD ROM
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- Synopsys for the Tote Bag
- Intel and IBM Microelectronics for Electronic Projection
- Texas Instruments for a Coffee Break
- Emerging Memory Technologies for a Coffee Break
- Tanner EDA for the Lanyards

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AIRPORT TRANSPORTATION

The Caribe Royale is 18 miles from the Orlando International Airport. Mears Shuttle Service provides shuttle service from the airport to the hotel. For transportation from the airport to the hotel, go to the Mears Desk, one floor below baggage claim. Vans depart the airport every 20 – 40 minutes. For transportation from the hotel to the airport, call Mears at (407) 839-1570, 24 hours before your flight to make a reservation. The cost is approximately \$17.00/one way or \$29.00/round-trip. Taxi service is also available from the airport at an estimated cost of \$40 – 50.00 one way.

BADGES

Badges are required for admittance to all sessions and the exhibit hall. Please wear your badge at all times while attending the conference so that you will not be delayed entry to a session.

FOR FURTHER INFORMATION CONTACT

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April 1, 2005
Paper Submission Deadline

September 18 - 21, 2005
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Circuits Conference
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