

Welcome to the IEEE Custom Integrated Circuits Conference

Welcome to the 25th annual Custom Integrated Circuits Conference, CICC 2003. As you have noticed, the CICC has moved to the fall to better accommodate the design community's needs. Since this is our 25th Anniversary, several special events are planned to celebrate including: a keynote presentation by Dr. Robert Lucky on technology in the midst of the telecom turmoil, a conference luncheon with guest speaker Dr. Tsugio Makimoto, an expanded technical program with 27 technical sessions, three evening panels, and several social events. The CICC is the leading international conference for integrated circuit development where first time advancements are published. CICC provides a unique forum for all individuals involved with IC development to meet and share information about the most recent advances in system architectures, circuit and computer-aided design, and process technology. CICC's goal is to offer attendees a total educational experience balanced between paper presentations, exhibits, panels, tutorials and interesting networking events. You are cordially invited to help us celebrate our 25th Anniversary and participate in CICC 2003, located in San Jose, California at the DoubleTree Hotel

The conference starts with four educational sessions on Sunday, September 21st, 2003. These sessions are taught by practicing experts working at the leading edge of their field. The topics for these sessions are: Advanced RF, Advanced Data Converters, High-Performance and Low-Voltage Design, and SoC/Mixed Signal/RF Design, Verification and Test.

On Monday morning, the technical program begins with the keynote speaker, Dr. Robert Lucky, author of the bimonthly "Reflections" column in IEEE Spectrum Magazine. Dr. Lucky's discussion of technology in the midst of the telecom turmoil will provide a lively opening for the expanded CICC technical program.

The technical program offers exceptional technical papers that provide the latest and most significant developments in the IC industry. This year, more than 380 technical papers were submitted, of which 147 were selected and organized into 27 sessions. These high quality and informative papers address topics including: Wireless & Wired Communications, Analog, Custom & Low Power Circuits, System-on-a-Chip/IP, Simulation & Modeling, Signal & Data processing, Embedded Memories, Programmable Devices, Fabrication, and Test & Reliability. These technical sessions are highlighted by invited and tutorial papers presented by leading experts from industry and academia. New for this year's CICC are Emerging Technologies sessions which feature very interesting invited papers on a wide range of topics.

Monday afternoon the Exhibitor Preview Sessions kick off the opening of the Exhibits Hall. Here many of our Exhibitors will present overviews of new products and services. During the Monday evening Exhibitors' Reception you will find refreshments and professional networking at its very best! As always, our exhibits area will include booths and software demonstrations from prominent corporations in the industry.

You will not want to miss this year's conference luncheon. Our honored guest speaker, Dr. Tsugio Makimoto, Corporate Advisory, Sony Corporation will address the critical role played by chip technology in robotic development. This promises to be a fascinating and educational experience.

On Tuesday evening, three spirited panel discussions are scheduled featuring experts who are sure to offer strong opinions on the three topic areas: Outsourcing, analog device modeling, and technology vs. product developer needs. This year, for the first time ever at an IEEE conference, we will include a panelist selected from the audience for the panel "Technology: Falling Short of Product Developer Needs?"

We extend our thanks to all the authors who spent many hours on the preparation of their submitted papers. We also wish to thank the CICC Technical Program Committee and our dedicated conference staff for all of their hard work and support. It is their diligent efforts that keep CICC as the best place to discover the latest in integrated circuit innovations, newest product announcements, and to debate the most effective business strategies. See you in San Jose!

EDUCATIONAL SESSIONS

Sunday, September 21

Chairperson: Doug Garrity, Motorola

**Ed. Session 1 - Advanced RF:
From Devices to Systems**
Oak Ballroom, Sunday, September 21

Organizer: Larry Nagel, Omega Enterprises

Co-organizer: Francesco Svelto, Università di Pavia

E1-1 RF Performance and Modeling of CMOS Devices
8:00-9:50 R. van Langevelde, Philips Research Laboratories

Continuous downscaling of CMOS process technologies has resulted in a strong improvement in the RF performance of MOS devices. Consequently, CMOS has become a viable option for analog RF applications and RF system-on-a-chip. In order to allow for versatile RF circuit design in CMOS technologies, a number of issues, which traditionally get little or no attention in compact MOS modeling for digital or low-frequency analog circuit design, have to be taken into account. These issues include power gain, output impedance and bulk resistance, input impedance and gate resistance, non-quasi-static (or transit time) effects, power gain, noise, 1/f (or flicker) noise, thermal noise, induced gate noise and distortion.

This presentation focuses on the discussion of these issues for CMOS devices, in addition an overview will be given of the present state-of-the-art of compact modeling. This part will be followed by a discussion, using both simulations and measurements, of layout effects on the RF performance of CMOS devices. Finally, the performance and modeling of passive devices such as varicaps (or varactors) and inductors will be discussed.

E1-2 RFIC Receiver Circuits
10:10-12:00 John R. Long, Delft University of Technology

This lecture addresses the design of RFIC receiver circuits in CMOS and BiCMOS technologies from antenna to base-band. Major IC building blocks such as low-noise preamplifiers, down-converting mixers, voltage-controlled oscillators, image-reject down-converters and frequency scalars are considered. Technology evaluation for RF performance, selection of an appropriate circuit topology and the relationship between the circuit and system specifications as preliminary steps in the design process are outlined. The advantages and limitations of on-chip inductors, transformers and other passives available for RFIC work are discussed. Issues in modeling, simulation and circuit design based on the passive and active components available in standard IC design kits and tools are highlighted within the context of each building block. Co-integration and evaluation of receiver blocks are described, with emphasis on topics such as physical layout, package parasitics, off-chip matching, test fixtures and chip evaluation at RF.

E1-3 Key Issues in Transmitter Blocks
1:00-2:50 Earl McCune, Tropian Inc.

This presentation will focus on higher order issues for transmitter blocks not generally seen in textbooks. These are grouped into three areas: 1) effects of error sources in quadrature modulators and demodulators, 2) issues with on-channel RF signal processing (direct conversion/modulation), and 3) successful implementation of RF circuitry in the presence of local digital CMOS.

E1-4 From RF System to Silicon
3:10-5:00 Asad A. Abidi, University of California, Los Angeles

Expertise in RF circuits traditionally concentrates on the design and optimization of individual circuit blocks, such as better amplifiers, mixers, or oscillators. However, in the context of single-chip transceivers, the importance of the right receiver or transmitter architecture usually has a much greater impact on performance and power consumption than improvements in any given circuit. Without sufficient thought given to architecture, even the best circuits may lead to an inferior end result. The practical problems of on-chip interconnections and buffering at RF are often overlooked.

In this presentation, we will use various examples to show this process at work. The examples include an adaptive 2.4 GHz linear receiver for wireless LAN, a 900 MHz receiver and transmitter for GSM, and a 900 MHz very low power receiver for paging usage.

**Ed. Session 2 - Advanced Data Converter
Design Techniques**

Fir Ballroom, Sunday, September 21

Organizer: Pat Rakers, Motorola
Co-organizer: Don Thelen, AMI Semiconductor

E2-1 Introduction to Sigma-Delta Data Converters
8:00-9:50 Matt Miller, Motorola Labs

As IC process technologies have progressed, noise-shaping data converters, already known for their superior linearity performance, have steadily overtaken wider bandwidth applications previously dominated by Nyquist rate data converters. This talk will start with the fundamental concepts of noise-shaping converters and also cover some of the more recent architectural innovations that have led to the dominance of the sigma-delta data converter as the choice for a wide variety of high resolution-bandwidth applications including wireless receivers. A brief case study of a multi-bit sigma-delta ADC design for a receiver application will help to illuminate some of the key considerations involved in noise-shaping data-converter circuit design.

E2-2 Continuous-time delta-sigma ADCs
10:10-12:00 Kathleen Philips, Philips Research

Most of present-day delta-sigma ADCs are time-discrete, yet interest in continuous-time converters has grown rapidly. After a brief introduction on delta-sigma fundamentals, differences between continuous-time and discrete-time implementation are explained. Continuous-time designs have the capability of lower noise (no kT/C) and higher conversion bandwidth than discrete-time implementations. Several examples show that power consumption (normalized to performance) of continuous-time delta-sigma ADCs is amongst the lowest reported for data converters. We analyze design challenges such as sensitivity to parameter spread, jitter, excess loop delay, memory effects, etc. and present -or refer to- some solutions. Finally, some advanced application examples exploiting the specific characteristics of the time-continuous implementation are discussed.

E2-3 Device Mismatch for Data Converter Design-
1:00-2:50 Patrick Drennan, Motorola

Device matching is the heart of precision analog design. Ironically, the significance of analog has grown more prominent in the "digital" age, due, in part, to data converters. Mismatch variance is inversely proportional to device area, which means that well matched devices come at the expense of larger die, parasitic capacitance and power consumption. Even more expensive, advanced techniques such as laser trimming, memory-stored mismatch correction, and mismatch shaping do not lessen the desire for the best intrinsically matched devices. A physical description of mismatch variation will establish the foundation for this presentation. We'll walk through the evolutionary steps of mismatch model development and discuss how mismatch fits into the big picture of statistical device variation. The majority of the presentation will approach mismatch from the design perspective, concentrating on MOSFETs, capacitors, and resistors. This presentation will discuss device sizing, bias dependencies, metal routing over devices, gradient effects, gate protect diodes, dummy devices, and measurement and characterization issues.

E2-4 Practical Aspects of Nyquist-Rate Switched-Capacitor ADCs
3:10-5:00 David Nairn, Analog Devices

System and circuit level issues for switched-capacitor (SC), Nyquist rate analog-to-digital converters (ADCs) will be discussed. After a brief review of the common SC ADC architectures, flash, successive approximation, cyclic and pipelined, the tradeoffs between the architectures will be considered. Then, system-level issues such as noise and accuracy in conjunction with their effects on partitioning and scaling will be considered for the ADCs. Following this, the discussion will focus on specific circuit and design issues related to sub-components such as switches, capacitors, op amps and comparators. Where appropriate, example circuits will be analyzed and good layout practices will be considered.

Ed. Session 3 - High-Performance and Low-Voltage Design Challenges and Techniques

Pine Ballroom, Sunday, September 21

Organizer: Un Koon Moon, Oregon State University
Co-organizer: Steffen Rochel, Cadence Design Systems

E3-1 Low-Power Circuit Design in SOI Technology **8:00-9:50** Andrew Marshall, Texas Instruments, Inc.

Silicon on insulator (SOI) technology has become an important frontier in the progression of the development of semiconductor electronics. Digital circuitry is well understood, and steady advances in the application of analog designs are being made. Performance improvement, reduced power, component isolation and an increase in circuit density are some of the touted benefits. There are, however, tradeoffs, including bipolar leakage effects, thermal issues, transistor matching difficulties and history and kink effects for some SOI technologies. A brief overview of the major SOI process options is given and comparison is made between SOI and bulk material. The various SOI types, especially partially depleted, fully depleted, FinFET and double-gate structures are discussed. The challenge of modeling SOI devices is explored and some concepts for successful SOI circuit layout are introduced, including a discussion of various options for the reduction of thermal self-heating effects. The development of circuits for low voltage and low power are discussed for analog and digital applications. By way of conclusion, trends in SOI development are addressed.

E3-2 High Performance and Leakage Tolerant **10:10-12:00 Circuit Technologies** Ram Krishnamurthy, Intel Corporation

Continued demand for high-performance in high-end server and desktop platforms as well as mobile/handheld multimedia platforms has imposed three primary obstacles: (i) a power-constrained scenario, (ii) aggravated transistor leakage currents, and (iii) a worsening on-chip interconnect scaling trend. This tutorial examines some of these primary challenges and the associated key paradigm shifts that will be required in future microprocessors and DSPs. Circuit design techniques to combat (i) increasing switching and active leakage power consumption while sustaining high system performance, (ii) poor leakage tolerance and robustness of register file and array bitlines, and (iii) a worsening global on-chip interconnect scaling trend are presented. Examples of some of the techniques and their results that will be described: (i) Dual-supply and dual-threshold voltage datapath and clocking design for switching and active leakage reduction, and associated static-power-free write-port latches and level converter techniques; (ii) single-rail and conditional/burn-in tolerant dynamic circuit design styles for leakage noise tolerance and process parameter variation tolerance; (iii) pseudo-static, split-decoder, and self-reverse biased register file bitline design techniques with aggressive bit-line active leakage control; (iv) low peak-current static and transition-encoded driver design techniques for high-speed on-chip buses; (v) energy-efficient sparse-tree ALU and multiplier circuit techniques to mitigate power density/thermal hotspots; and (vi) special-purpose DSP hardware accelerator circuits targeted for high-performance multimedia and wireless applications.

E3-3 Emerging Memory Technologies **1:00-2:50** Sreedhar Natarajan, MoSys Incorporated

Semiconductor memories have been around for well over 25 years and have increased in density from the early 1K's to the current 4Gb in 2003. Technological trends today are approaching fundamental limits of physics - hence the need to evaluate future emerging memory technologies. Ideal characteristics of any future universal unified memory technology should be to meet the performance of an SRAM, density of a DRAM and nonvolatility (like Flash). So far in the non-volatile space, the market is dominated by flash memories based on relatively standard silicon design processes, but a huge range of more exotic options is being explored. The industry is looking at a wide range of novel memory technologies, including Polymer Memory, Ovionics Unified Memory (OUM), Magnetoresistive RAM (MRAM), MEMS and ferro-electric RAM (FeRAM), Carbon nanotubes and Thyristor RAMs. Each has its own characteristics which makes it more or less suitable for particular applications but only one or two will make it as a mainstream technology. Memory dominance on SoCs continues to increase and hence tomorrow's high-quality SoCs require high-quality memory today. The emerging memory technology should be (1) a universal memory (2) a process solution (replacement of SRAM, DRAM and Flash) (3) suitable for the ASIC market. The emerging memory technology should also be suitable for the SoC market since silicon foundries implement

SoC initiatives. The technology that is most economical and satisfies the density and performance requirements (universal) will be the one most widely accepted. This tutorial will highlight all the emerging memory technologies being researched today and conclude on which is currently closest to becoming mainstream.

E3-4 Low-Power Circuit Technologies
3:10-5:00 Kaushik Roy, Purdue University

The tremendous growth of the semiconductor industry is fueled by scaling of technology following Moore's Law. However, as we enter the nanometer regime, leakage current is becoming one of the main concerns for designers. Circuit designers have to work hand in hand with device designers to deliver high-performance yet low-power and noise-tolerant systems. This talk will consider different leakage mechanisms in nanometer scale devices and propose device architecture and circuit/CAD solutions for leakage-tolerant logic and memories for scaled technologies.

Ed. Session 4 – Hands on for SoC/Mixed-Signal/RF: Design, Verification and Test

Cedar Ballroom, Sunday, September 21

Organizer: Albert Wang, Illinois Institute of Technology
Co-organizer: David Allee, Arizona State University

E4-1 SoC and ASIC Functional Verification Methods
8:00-9:50 Anders Nordstrom, Elliptic Semiconductor

The tutorial gives an overview of the digital ASIC and SoC verification methods in use in the industry today as well as a brief history of the evolution of functional-verification methods from simulation to formal methods. Assertion Based Verification and intelligent testbenches that are the latest verification trends are explained in relation to other advanced verification methods. The concept of design and verification assertions, where they are used and how they are verified, is explored. Several examples of different types of assertions will be given and the most common assertion formats (pseudo comments, Open Verification Library and Sugar) will be explained.

E4-2 Modeling and Simulation Issues in Phased-Locked Systems
10:10-12:00 Behzad Razavi, University of California, Los Angeles

This presentation covers passive and active device models for PLL design; PLL modeling for fast simulation; simulation of phase noise and jitter; bang-bang loop modeling issues; modeling and simulation of frequency synthesizers and clock and data recovery circuits; and behavioral versus transistor-level modeling.

E4-3 RF Integrated Circuit Design Using Parasitic-Aware Optimization Methods
1:00-2:50 David Allstot, University of Washington

In RF integrated circuit design, efforts are aimed at the realization of true single-chip radios with few, if any, off-chip components. Perhaps ironically, the on-chip passive components required for RF integration pose more serious challenges to SOC integration than the active devices. This is not surprising since modern digital IC designs are dominated more by interconnect than active device characteristics. The co-integration of active and passive devices in RF IC design represents a daunting design and manufacturing challenge. Unfortunately, conventional mixed-signal design techniques simply do not work well for RF designs because parasitics associated with passive elements and the package effectively de-tune them. Hence, dealing with parasitics as part of the design process is an essential goal of the parasitic-aware RF circuit synthesis approach. It comprises three key components: The circuit simulator is HSPICE or SPECTRE-RF. A compact model generator provides the parasitic modeling function. The optimization core uses adaptive simulated annealing with tunneling or particle swarm optimization. The main goal of this presentation is to describe the parasitic-aware RF circuit design methodology and illustrate its application to a variety of practical examples including noise-figure minimization in low-noise amplifiers, intercept point maximization in mixers, phase-noise minimization in voltage-controlled oscillators, and power output and efficiency maximization in power amplifiers.

E4-4 Test Cores for On-Chip Measurements

3:10-5:00 Gordon Roberts, McGill University

With the growing complexity of integrated circuits reaching the tens-of-million-plus transistor scale, electronic component and system manufacturers are moving towards increased usage of third-party electronic component wares (cores). Besides the obvious need for standards to assist in their integration, the need for individual verification and test is paramount to overall product success. From a digital design perspective, the appropriate design and test methodologies are, for the most part, already in place. Scan techniques will continue to be used to move test information about a complex IC, regardless of the core origin. In contrast, no simple method exists in which to move analog information around on an IC without serious degradation of its signal-to-noise ratio. This limits the solutions to carefully crafted test buses, on-chip digitizers and on-chip analog signal generators. Consideration towards using existing chip resources, such as a DSP-core, can simplify the design of specialized test hardware. In this talk, we shall describe these potential mixed-signal/analog test techniques for cores consisting of A/Ds, D/As, CODECs, PLLs, and RF transceivers. Results from IC experiments will be provided as much as possible.

EXHIBITS

CICC once again combines its outstanding technical program with a variety of exhibitors. Exhibits will include displays and demonstrations by semiconductor manufacturers, software tool suppliers, design service houses, and leading electronics industry publications. The Exhibit Hall will be the site for Monday's Exhibitors' Reception and Tuesday evening's Happy Hour.

Partial Listing of Exhibitors:

Aeroflex	Neonlinear, Inc.
Analog Design Automation	Prentice Hall
Anasift Technology	Sagantec
Austriamicrosystems USA, Inc.	Sandwork Design, Inc.
Cambridge University Press	Silvaco International
ChipMD	Synopsys, Inc
Kluwer Academic Publishers	Wiley
NASSDA	

EXHIBIT HOURS

Donner Ballroom

Monday, September 22

2:00 pm - 8:00 pm – Exhibits Open
1:00 pm - 2:00 pm Exhibitor Preview Session
5:30 pm - 8:00 pm Exhibitors' Reception

Tuesday, September 23

2:00 pm - 7:00 pm – Exhibits Open
5:30 pm - 7:00 pm Happy Hour

EXHIBITORS' PREVIEW SESSIONS

Monday, September 22, 1:00 pm - 2:00 pm

PREVIEW SESSION 1, Monterey Room

- 1:00** **Analog Design Automation** – Methodology for Designer-controlled Front-end Optimization for Analog, Mixed-Signal & Custom ICs
- 1:20** **ChipMD** – Design for Yield with Deterministic Analysis
- 1:30** **Sagantec**- TBD

PREVIEW SESSION 2, Carmel Room

- 1:00** **NASSDA** – Dynamic Nanometer Analysis
- 1:20** **Synopsys** Synopsys' Newest Advances in Mixed-Signal Verification
- 1:40** **Aeroflex UTMC** – Aeroflex Mixed-Signal Standard Product and SoC Solutions
- 1:50** **Sandwork Design** – SPICE Explorer-A Circuit-Level Debugging Environment

TECHNICAL SESSIONS

Monday, September 22 - Wednesday, September 24

Session 1 – Keynote Presentation

Oak/Fir Ballroom, Monday Morning, September 22

8:00am Welcome/Opening Remarks
Awards Presentations
Keynote Speaker Introduction
Phil Diodato, General Chairman

8:20am KEYNOTE ADDRESS
“Technology in the Midst of Telecom Turmoil” Dr. Robert Lucky,
author of the bimonthly “Reflections” column in IEEE Spectrum
Magazine

Industrial support for telecom research has fallen in the wake of the telecom crash, as has spending for new technology products. Yet there is exciting new technology waiting to be adopted, particularly in wireless, optics, and networking. Whether this new technology can be the savior for the industry or only exacerbate the business model problems remains to be seen. Moreover, the arguments that currently rage over telecom regulation, spectrum management, and copyright control will heavily impact whatever phoenix arises from the ashes of today's industry firestorm. This talk is a survey of the current landscape from the point of view of a technologist hoping to see a new world emerge in which bandwidth is plentiful and cheap, access is mobile and ubiquitous, information is freely exchanged, and research is well supported.

Dr. Lucky, an IEEE Fellow, is well known for his groundbreaking work in adaptive equalization at AT&T Bell Labs. He has also served as the Executive Director of Communication Sciences Research Division at Bell Labs, Chairman of the Scientific Advisory Board for the United States Air Force, and has received numerous honorary doctorates and industry awards including the Marconi Award for his contribution to data communications. Dr. Lucky's presentation will provide a lively opening to the CICC technical program.



Session 2 – Analog Filters

Oak Ballroom, Monday Morning, September 22

Chair: David Allee Co-Chair: Yusuf Haque

Analog filters using continuous time and switched capacitor techniques with center frequencies up to 28 MHz are demonstrated. Advancements include linearity improvements, new tuning techniques, and lower power dissipation.

10:00 am Introduction

10:05 am Automatic Tuning of RC Filters and Fast Automatic
2-1 Gain Control for CMOS Low-IF Transceiver, T. Oshima, K. Maio, W. Hioe, Y. Shibahara, T. Doi, Hitachi Ltd., Tokyo, Japan

10:30 am OTA Linearity Enhancement Technique for High
2-2 Frequency Applications with IM3 Below -65dB, A. Lewinski and J. Silva-Martinez, Texas A&M University, College Station, TX

10:55 am A 58dB SNR 6th Order Broadband 10.7 MHz SC
2-3 Ladder Filter, J. Silva-Martinez*, J. Aducci** and M. Rocha-Perez*#, *Texas A&M University, College Station, TX, **Texas Instruments, Dallas, TX and #INAOE and CINVESTAV, Guadalajara, Mexico

11:20 am 2-4 A 28-MHz Wide-Band Switched-Capacitor Bandpass Filter with High Attenuation, K.W.H. Ng and H.C. Luong, Hong Kong University of Science and Technology, Kowloon, Hong Kong

11:45 am 2-5 A Power Efficient Channel Selection Filter / Coarse AGC With No Range Switching Transients, Y. Palaskas, Y. Tsvividis* and **V. Bocuzzi, Intel Labs, Hillsboro, OR, *Columbia University, New York, NY and **Agere Systems, Allentown, PA

Session 3 – SoC Design, Methodology, and Infrastructure
Fir Ballroom, Monday Morning, September 22

Chair: Henry Chang Co-Chair: Rakesh Patel

This session presents three state-of-the-art SoCs and discusses the design flows used for these multi-million-gate wireline and wireless ICs.

10:00 am Introduction

10:05 am 3-1 The iFlow Design Factory Infrastructure for a 17M-gate, 0.13 μ m, 333MHz Design, (Invited) G.-E. Descamps and S. Bagalkotkar, Silicon Access Networks, San Jose, CA

10:55 am 3-2 Design and Development of the First Single-Chip Full-Duplex OC48 Traffic Manager and ATM SAR SoC, A. Khan+, K. Patel, A. Aurora*, A. Raza*, B. Parruck*, A. Bagchi*, A. Ghosh*, B. Litinsky*, E. Hong*, E. Zhao*, J. Ngo*, K. Ko*, L. Singh*, P. Arnaudov*, P. Wu*, R. Ramakrishnan*, R. Zecharia*, S. Channabasappa*, S. Kumar*, S. Wattal*, T. Wang*, U. Joshi*, Z. Golan*, Z. Luo*, D.-N. Le+, I. Ahmed+, F. Chiu+, K.Y. Chow+, H. Furuzono+, D. Ge+, M. Li+, M. Mueller+, S. Nguyen+, T. Nguyen+, J. Saito+, J. Shen+, A. Todesco+, A. Tsou+, D. Wang+, S. Yang+, J. Yu+ and Z. Zhong+, *Azanda Network Devices, Inc., +Cadence Design Systems, Inc.

11:20 am 3-3 The Intel® PXA800F Wireless Internet-On-a-Chip Architecture and Design, D. Krishnaswamy, R. Stevens, R. Hasbun, J. Revilla and C. Hagan, Intel Corporation, Folsom, CA

Session 4 – Programmable Logic: New Roads to Low Cost

Pine Ballroom, Monday Morning, September 22

Chair: Vaughn Betz Co-Chair: Steve Wilson

In today's tight economic market, cost is everything. Programmable devices of all stripes are evolving to achieve reductions in silicon, design, and mask costs.

10:00 am Introduction

10:05 am 4-1 SoC Implementation Issues for Synthesizable Embedded Programmable Logic Cores, J.C.H. Wu, V. Aken'Ova, S. Wilton and R. Saleh, University of British Columbia, Vancouver, Canada

10:30 am 4-2 Cyclone™: A Low-Cost, High-Performance FPGA, P. Leventis*, M. Chan, M. Chan*, D. Lewis*, B. Nouban, G. Powell, B. Vest, M. Wong, R. Xia and J. Costello, Altera Corporation, San Jose, CA and * Toronto, Canada

- 10:55 am 4-3 Regular Logic Fabrics for a Via Patterned Gate Array (VPGA)**, K.Y. Tong, V. Kheterpal, V. Rovner, L. Pileggi, H. Schmit and R. Puri*, Carnegie Mellon University, Pittsburgh, PA and *IBM T.J. Watson Research Center, Yorktown Heights, NY
- 11:20 am 4-4 Leakage Power Analysis of a 90nm FPGA**, T. Tuan and B. Lai*, Xilinx Research Labs, San Jose, CA and *University of California, Los Angeles, CA
- 11:45 am 4-5 Architecture of Datapath-Oriented Coarse-Grain Logic and Routing for FPGAs**, A. Ye, J. Rose and D. Lewis, University of Toronto, Toronto, Canada

Session 5 – Timing Recovery
Cedar Ballroom, Monday Morning, September 22

Chair: Jafar Savoj Co-Chair: Vincent Von Kaenel

This session addresses practical issues in the design of multi-gigabit clock and data recovery circuits and presents novel low-power implementations in CMOS technology.

- 10:00 am Introduction**
- 10:05 am 5-1 Analysis of Timing Recovery for Multi-Gbps PAM Transceivers**, C.-K.K. Yang and K.-L.J. Wong, University of California, Los Angeles, CA
- 10:30 am 5-2 A 10-Gb/s CMOS Clock and Data Recovery Circuit with an Analog Phase Interpolator**, R. Kreienkamp, U. Langmann and C. Zimmerman*, Ruhr Univ., Bochum, Germany and *Toshiba Electronics, Dusseldorf, Germany
- 10:55 am 5-3 A 33mW 8Gb/s CMOS Clock Multiplier and CDR for Highly Integrated I/Os**, H.-T. Ng, M.-J. E. Lee, R. Farjad-Rad, R. Senthinathan, W. J. Dally*, A. Nguyen, R. Rathi, T. Greer, J. Poulton, J. Edmondson, J. Tran, Velio Communications Inc., Milipitas, CA and *Stanford Univ., Stanford, CA
- 11:20 am 5-4 A 10-Gb/s CMOS Clock and Data Recovery Circuit Using a Secondary Delay-Locked Loop**, W. Rhee, H. Ainspan, S. Rylov, A. Rylyakov, M. Beakes, D. Friedman, S. Gowda and M. Soyuer, T.J. Watson Research Center, Yorktown Heights, NY

Session 6 – Modeling for RF Design
Sierra Ballroom, Monday Morning, September 22

Chair: Hong-Ha Vuong Co-Chair: Elliot Gould

This session discusses optimized design and the use of active and passive components for RF applications along with modeling methodology for harmonic/balance and spectral spreading.

- 10:00 am Introduction**
- 10:05 am 6-1 MOSFET HF Distortion Behavior and Modeling for RF IC Design**, T.-Y. Lee and Y. Cheng, Skyworks Solutions, Irvine, CA

- 10:30 am** **Non-Linear Transmission Lines for Pulse Shaping in Silicon**, E. Afshari and A. Hajimiri, California Institute of Technology, Pasadena, CA
6-2
- 10:55 am** **Differentially-Shielded Monolithic Inductors**, T.S. Cheung, J.R. Long*, K. Vaed**, R. Volant**, A. Chinthakindi**, C.M. Schnabel**, J. Florkey**, Z.X. He**, K. Stein**, Univ. of Toronto, Ont., Canada, *Delft Univ. of Tech., Netherlands and **IBM Microelectronics, Hopewell Junction, NY
6-3
- 11:20 am** **A Comparison of Non-Quasi-Static and Quasi-Static Harmonic Balance Implementations for Coupled Device and Circuit Simulation**, Y. Hu and K. Mayaram, Oregon State University, Corvallis, OR
6-4
- 11:45 am** **Analysis of Spectral Spreading in a Phase-Modulated System for 1.75-GHz GSM RF Transmitter Design**, H. Shin, B. Walker, D. Pan, J. Dunworth and J. Jaffee, Qualcomm Inc., San Diego, CA
6-5
- 12:10 am** **Statistical Analysis of Integrated Passive Delay Lines**, B. Analui and A. Hajimiri, California Institute of Technology, Pasadena, CA
6-6

<p>Session 7 – Oversampled Data Converters Oak Ballroom, Monday Afternoon, September 22</p>
--

Chair: Don Thelen Co-Chair: Pat Rakers

In this session, Delta Sigma modulation is used in a diverse group of circuits including low-pass, bandpass and continuous time data converters.

- 2:00 pm** **Introduction**
- 2:05 pm** **Cascaded Noise-Shaping Modulators for Oversampled Data Conversion**, (Tutorial) Bruce Wooley, Stanford University, Stanford, CA
7-1
- Through the exchange of resolution in time for that in amplitude, noise-shaping sigma-delta modulators facilitate the realization of precision A/D and D/A converters in scaled CMOS VLSI technologies. Cascaded architectures are a robust means of extending the performance of such modulators to signal bandwidths of several megahertz since their design is straightforward and they are immune to the stability issues that accompany the design of high-order modulators employing a single quantizer. To meet the performance demands of emerging communications applications, distributed noise-shaping and multilevel quantization can be used to significantly lower the oversampling ratio needed to achieve a specified precision, thus increasing the signal bandwidth that can be digitized within the constraints of a given technology. It is thereby possible to encode signals with bandwidths of several megahertz centered at dc or at intermediate frequencies of tens of megahertz. Digital cascaded noise shaping modulators can be used for D/A conversion, and means have been found to combine such architectures with semi-digital reconstruction filtering. This presentation reviews the use of cascaded noise-shaping modulator architectures for both A/D and D/A conversion and describes some of the circuit techniques employed in their implementation.
- 2:55 pm** **A 16-Bit, 5MHz Multi-Bit Sigma-Delta ADC Using Adaptively Randomized DWA**, Y.-I. Park, S. Karthikeyan, W.M. Koe, Z. Jiang and T.-C. Tan, Texas Instruments, Dallas, TX
7-2
- 3:20 pm** **A 1.8-V 3-MS/s 13-Bit Delta-Sigma A/D Converter with Pseudo Data-Weighted-Averaging in 0.18- μ m Digital CMOS**, A.A. Hamoui and K. Martin, University of Toronto, Toronto, Canada
7-3

- 3:45 pm Break**
- 4:00 pm 7-4 A 92 MHz, 80 dB Peak SNR SC Bandpass Sigma-Delta Modulator Based on a High GBW OTA with no Miller Capacitors in 0.35 μ m CMOS Technology,** B. Thandri, J. Martinez, J. Rocha-Perez* and J. Wang, Texas A&M University, College Station, TX and *INAOE, Guadalajara, Mexico
- 4:25 pm 7-5 A 1.3-GHz IF Digitizer using a 4th-Order Continuous-Time Bandpass Delta-Sigma Modulator,** T. Kaplan*#, J. Cruz-Albrecht*, M. Mokhtari*, D. Matthews*, J. Jensen* and M.F. Chang#, *HRL Labs, Malibu, CA and #University of California, Los Angeles, CA
- 4:50 pm 7-6 A 942 MHz Output, 17.5 MHz Bandwidth, -70dBc IMD3 Sigma-Delta DAC,** S. Luschas, R. Schreier*, H.-S. Lee, Massachusetts Institute of Technology, Cambridge, MA and *Analog Devices, Inc., Wilmington, MA
- 5:15 pm 7-7 A 200-MHz Continuous-Time CMOS Delta-Sigma Modulator Featuring Nonlinear Feedback Control,** T. Zourntos, Texas A&M University, College Station, TX

<p>Session 8 – Next Generation RF Technologies Fir Ballroom, Monday Afternoon, September 22</p>
--

Chair: Edoardo Charbon Co-Chair: Nobuyuki Itoh

This session presents advanced designs and novel MEMS technologies for ultra-low-power and high-frequency operation. Cost effectiveness and reliability are shown for a variety of applications ranging from deep-space exploration to standard radio transceivers.

- 2:00 pm Introduction**
- 2:05 pm 8-1 High Performance RF-Filters Suitable for Above IC Integration: Film Bulk-Acoustic- Resonators (FBAR) on Silicon, (Invited)** R. Aigner, Infineon Technologies, Munich, Germany
- 2:55 pm 8-2 CMOS LC Oscillator using Variable Mean Frequency,** P.-H. Hsieh, J. Judy, and C.-K. K. Yang, University of California, Los Angeles, California
- 3:20 pm 8-3 A 1-V 2.4-GHz FSK Receiver with a Complex BPF and a Frequency Doubler in CMOS/SOI,** M. Ugajin and T. Tsukahara, NTT Microsystem Integration Labs, Kanagawa, Japan
- 3:45 pm Break**
- 4:00 pm 8-4 A Low Power PSK Receiver for Space Applications in 0.35- μ m SOI CMOS,** M.R. Yuce*, W. Liu***, J. Damiano*, B. Bharat*, P. Franzone* and N. Dogan#, *NC State University, Raleigh, NC, **University of California, Santa Cruz, CA and #NC A&T State Univ., Greensboro, NC
- 4:25 pm 8-5 A 4-91 GHz Distributed Amplifier in a Standard 0.12 μ m SOI CMOS Microprocessor Technology,** J.-O. Plouchart, J. Kim, N. Zamdmer, L.-H. Lu, M. Sherony, Y. Tan, R. Groves, R. Trzcinski, M. Talbi, A. Ray and L. Wagner, IBM Semiconductor Research and Development Center, Hopewell Junction, NY

4:50 pm **A Batteryless Wireless System with MTCMOS/SOI**
8-6 **Circuit Technology, (Invited)** T.Douseki, T. Tsukahara,
Y.Yoshida*, F.Utsunomiya* and N.Hama**, NTT Corp.,
Kanagawa, Japan, *Seiko Instruments Inc., Chiba, Japan
and ** Seiko Epson Corp., Nagano, Japan

Session 9 – Application-Specific Signal Processors
Pine Ballroom, Monday Afternoon, September 22

Chair: Dawn Fitzgerald Co-Chair: Masataka Matsui

This session presents advances in application-specific signal processing including wireless, image processing, codec and encryption techniques.

2:00 pm **Introduction**

2:05 pm **Trends and Challenges for Wireless Embedded**
9-1 **DSPs, (Invited)** L.T. Clark, Intel Corp., Chandler, AZ

2:55 pm **A 1.1W Single-Chip MPEG-2 HDTV CODEC LSI for**
9-2 **Embedding in Consumer-Oriented Mobile CODEC**
Systems. H. Iwasaki, J. Naganuma, Y. Nakajima, Y.
Tashiro, K. Nakamura, T. Yoshitome, T. Onishi, M. Ikeda,
T. Izuoka and M. Endo, NTT Corporation, Kanagawa, Japan

3:20 pm **A Sub-mW MPEG-4 Motion Estimation Processor**
9-3 **Core for Mobile Video Application.** J. Miyakoshi,
Y.Kuroda, M.Miyama, K. Imamura, H. Hashimoto and
M.Yoshimoto, Kanazawa University, Kanazawa, Japan

3:45 pm **Break**

4:00 pm **Visconti: Multi-VLIW Image Recognition Processor**
9-4 **Based on Configurable Processor,** J. Tanabe, Y.
Taniguchi, T. Miyamori, Y. Miyamoto, H. Takeda, M.
Tarui, H. Nakayama, N. Takeda, K. Maeda and M. Matsui,
Toshiba Corporation, Kanagawa, Japan

4:25 pm **A Fully Programmable CMOS Block Matrix**
9-5 **Transform Imager Architecture,** A. Bandyopadhyay
and P. Hasler, Georgia Institute of Technology, Atlanta, GA

4:50 pm **A 2.3Gb/s Fully Integrated and Synthesizable AES**
9-6 **Rijndael Core,** N.S. Kim, T. Mudge and R. Brown,
University of Michigan, Ann Arbor, MI

Session 10 – Nanodevices & Other Alternatives
to CMOS Scaling

Cedar Ballroom, Monday Afternoon, September 22

Chair: Albert Wang Co-Chair: Rakesh Kumar

Emerging technologies are described for the design and fabrication of novel device structures, offering potential solutions to the fast-approaching CMOS scaling limits.

2:00 pm **Introduction**

2:05 pm **MEMS for Telecommunications: Devices and**
10-1 **Reliability, (Invited)** C.-P. Chang, New Jersey
Nanotechnology Consortium, Murray Hill, NJ

2:55 pm 10-2 **Three Dimensional CMOS Devices and Integrated Circuits, (Invited)** M. Jeong**, K. Guarini**, V. Chan*, K. Bernstein**, R. Joshi**, J. Kedzierski** & W. Haensch**, *IBM Semiconductor Research & Development Center, Hopewell Junction, NY and **Yorktown Heights, NY

3:45 pm **Break**

4:00 pm 10-3 **Amorphous Silicon TFT Circuit Integration for OLED Displays on Glass and Plastic, (Invited)** A. Nathan, K. Sakariya, A. Kumar, P. Servati, K.S. Karim, D. Striakhilev, A. Sazonov, University of Waterloo, Waterloo, Canada

4:50 pm 10-4 **Quantum-Dot Cellular Automata by Electric and Magnetic Field Coupling, (Invited)** G. Bernstein, University of Notre Dame, Notre Dame, IN

Session 11 – Advanced MOSFET Modeling

Sierra Ballroom, Monday Afternoon, September 22

Chair: Colin McAndrew Co-Chair: Laurence Nagel

These papers cover an extremely accurate surface-potential MOS model, models for SOI, STI stress, and ESD simulation, and a numerical model for DACs.

2:00 pm **Introduction**

2:05 pm 11-1 **SP: An Advanced Surface-Potential-Based Compact MOSFET Model (Invited)** G. Gilenblat, T.-L. Chen, X. Gu, H. Wang and X. Cai, The Pennsylvania State University, University Park, PA

2:55 pm 11-2 **A Unified Model for Partial-Depletion and Full-Depletion SOI Circuit Designs: Using BSIMPD as a Foundation**, P. Su, S.K.H. Fung, P. Wyatt*, H. Wan, M. Chan, A. Niknejad and C. Hu, University of California, Berkeley, CA and *MIT Lincoln Lab., Lexington, MA

3:20 pm 11-3 **A Scaleable Model for STI Mechanical Stress Effect on Layout Dependence of MOS Electrical Characteristics**, K.-W. Su, Y.-M. Sheu, C.-K. Lin, S.-J. Yang, W.-J. Liang, X. Xi*, C.-S. Chiang, J.-K. Her, Y.-T. Chia, C.H. Diaz and C. Hu*, Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan and *University of California, Berkeley, CA

3:45 pm **Break**

4:00 pm 11-4 **MCAST: An Abstract-Syntax-Tree Based Model Compiler for Circuit Simulation**, B. Wan, B.P. Hu, L. Zhou and C.-J.R. Shi, Univ. of Washington, Seattle, WA

4:25 pm 11-5 **A Verilog-A Compact Model for ESD Protection NMOSTs**, J. Li, S. Joshi and E. Rosenbaum, University of Illinois at Urbana-Champaign, Urbana, IL

4:50 pm 11-6 **An Accurate DAC Modeling Technique Based on Wavelet Theory**, J. Doyle, Y.J. Lee, Y.-B. Kim, Northeastern University, Boston, MA

Session 12 – DSP for Communications
Oak Ballroom, Tuesday Morning, September 23

Chair: Bryan Ackland Co-Chair: Ram Krishnamurthy

Advanced signal processing techniques are used to build communication ICs that extend capacity, provide greater resilience to errors, and deliver more reliable, and robust communications systems.

- 8:30 am Introduction**
- 8:35 am MIMO Signal Processing-The Next Frontier for
12-1 Capacity Enhancement, (Invited)** S. Mujtaba, Agere Systems, Allentown, PA
- 9:25 am APP Processing for High Performance MIMO
12-2 Systems**, D. Garrett, L. Davis*, S. ten Brink and B. Hochwald, Bell Laboratories, Lucent Technologies, Holmdel, NJ and *Sydney, Australia
- 9:50 am Break**
- 10:05 am An 8-User UMTS Channel Unit Processor for 3GPP
12-3 Base Station Applications**, C. Thomas*, T. Prokop*, M. Bickerstaff*, J. Niemasz**, P. Bernadac, P. Saintot, R. Laufer**, D. Bescher, R. Michel, B. Walker#, F. Derriennic, N. Burbau, E. Le Pape, J. Moreau, I. Cha**, S. Angioni#, K. Mhirs#, J. Lee**, P. Prat, G. Rogard, V. L'Aubin, D. Le Gall, C. Dagorn, D. Guillerm, P. Ragon, T. Goumis, M. Cooke*, B. Widdup*, G. Zhou*, C. Conan, P. Cabon, A. Carter#, C. Nicol*, P. Keevill# and P. Mankiewich**, Bell Laboratories, Lucent Technologies, Lannion, France, *North Ryde, Australia, **Whippany, NJ, #Swindon, UK
- 10:30 am Single-Chip FEC Codec Using a Concatenated
12-4 BCH Code for 10 Gb/s Long-Haul Optical Transmission Systems**, K. Seki, K. Mikami*, A. Katayama**, S. Suzuki, N. Shinohara*, M. Nakabayashi*, NEC Corp., *NEC Electronics Corp., **NEC Engineering, Ltd., Kanagawa, Japan
- 10:55 am Low Power Direct Digital Frequency Synthesizers
12-5 in 0.18 μm CMOS**, J. Langlois and D. Al-Khalili, Royal Military College of Canada, Kingston, Canada
- 11:20 am A 415 MHz Direct Digital Quadrature Modulator in
12-6 0.25- μm CMOS**, Y. Wu, D. Fu and A. Willson, University of California, Los Angeles, CA

Session 13 – Building Blocks for Broadband Communications

Fir Ballroom, Tuesday Morning, September 23

Chair: Un-Ku Moon Co-Chair: Kumar Lakshmi Kumar

Advancements in low-noise oscillator design and topologies are presented, along with emerging topics such as injection locking, ultra high-speed PRBS generation/checking, and an alternate signaling scheme.

- 8:30 am Introduction**
- 8:35 am An Integrated 10 GHz Quadrature LC-VCO in
13-1 SiGe:C BiCMOS Technology for Low-Jitter Applications**, F. Herzel, W. Winkler and J. Borngraeber, IHP, Frankfurt, Germany

- 9:00 am 13-2** **Techniques for In-Band Phase Noise Suppression in Re-Circulating DLLs**, S. Ye**, L. Jansson** and I. Galton*, *University of California, San Diego, CA and **Silicon Wave Inc., San Diego, CA
- 9:25 am 13-3** **A -107dBc, 10kHz Carrier Offset 2-GHz DLL-Based Frequency Synthesizer**, J. Zhuang, Q. Du and T. Kwasniewski, Carleton University, Ottawa, Canada
- 9:50 am** **Break**
- 10:05 am 13-4** **A Study of Injection Pulling and Locking in Oscillators, (Invited)** B. Razavi, University of California, Los Angeles, CA
- 10:55 am 13-5** **45-Gb/s SiGe BiCMOS PRBS Generator and PRBS Checker**, S. Kim, M. Kapur, M. Meghelli, A. Rylyakov, Y. Kwark and D. Friedman, IBM T.J. Watson Research Center, Yorktown Heights, NY
- 11:20 am 13-6** **A 2-Gb/s/pin Source Synchronous CDMA Bus Interface with Simultaneous Multi-Chip Access and Reconfigurable I/O Capability**, J. Kim, Z. Xu and M.F. Chang, University of California, Los Angeles, CA

<p>Session 14 – Directions in Process and Integration Pine Ballroom, Tuesday Morning, September 23</p>

Chair: David Sunderland Co-Chair: Larry Wissel

These invited papers present strategic directions in semiconductor process technology and integration, covering alternatives to pure CMOS scaling such as novel devices, system-on-chip processes and system-in-package solutions. Circuit designers will find these tutorials valuable in planning future products.

- 8:30 am** **Introduction**
- 8:35 am 14-1** **Advances in RF Packaging Technologies for Next-Generation Wireless Communications Applications (Invited)** L. Larson and D. Jessie*, Univ. of California, San Diego, CA and *Qualcomm, Inc., San Diego, CA
- 9:25 am 14-2** **SiGe BiCMOS Technology for Communication Products, (Invited)** M. Racanelli and P. Kempf, Jazz Semiconductor, Newport Beach, CA
- 9:50 am** **Break**
- 10:05 am 14-3** **Ultra-Thin Silicon-on-Sapphire Component Technology for Short Reach Parallel Optical Interconnects, (Invited)** C. Kuznia, J. Ahadian, M. Englekirk, M. Wong, J. Richaud, M. Pendleton, D. Pommer and R. Reedy, Peregrine Semiconductor Corp., San Diego, CA
- 10:30 am 14-4** **Scaling Beyond the 65 nm Node with FinFET-DGCMOS, (Invited)** E. Nowak, T. Ludwig*, I. Aller*, J. Kedzierski**, M. leong**, B. Rainey, M. Breitwisch, V. Gernhoefer*, J. Keinert* and D. Fried, IBM Microelectronics Division, Essex Junction, VT, *IBM Systems Group, Boeblingen, Germany and **IBM T.J. Watson Research Center, Yorktown Heights, NY
- 10:55 am 14-5** **Foundry Technology for 130nm and Beyond SoC, (Invited)** D.D. Tang, C.H. Diaz, C.P. Chao, H.M. Hsu, C.Y. Lee, C.S. Chang, Y.T. Chia, M.T. Yang and J.Y.-C. Sun, Taiwan Semiconductor Manuf. Co., Hsinchu, Taiwan

Session 15 – Design and Modeling Challenges
Cedar Ballroom Tuesday Morning, September 23

Chair: Stephen Rochel Co-Chair: Hidetoshi Onodera

Aggressive scaling poses new design and modeling challenges. This session starts with an overview of DSM design issues followed by presentations related to substrate noise analysis and optimization in mixed-signal designs.

- 8:30 am Introduction**
- 8:35 am Design and Modeling Challenges for 90 NM and 50**
15-1 NM, (Invited) V. Gerousis, Infineon Technologies,
Munich, Germany
- 9:25 am Strategies for Simulation, Measurement and**
15-2 Suppression of Digital Noise in Mixed-Signal
Circuits, B. Owens, P. Birrer, S. Adluri, R. Shreeve, S.
Arunachalam, H. Habal, S. Hsu, A. Sharma, K. Mayaram
and T. Fiez, Oregon State University, Corvallis, OR
- 9:50 am Break**
- 10:05 am Analyzing the Impact of Supply and Substrate**
15-3 Noise on Jitter in Gb/s Serial Links, S. Ramaswamy,
Texas Instruments Inc., Dallas, TX
- 10:30 am A Substrate Noise Analysis Methodology for**
15-4 Large-Scale Mixed-Signal ICs, W.K. Chu, N. Verghese,
H.-J. Cho, K. Shimazaki*, H. Tsujikawa*, S. Hirano*, S.
Doushoh*, M. Nagata**, A. Iwata#, T. Ohmoto#, Cadence
Design Systems, San Jose, CA, *Matsushita Electric
Industrial Co., Kyoto, Japan, **Kobe University, Kobe,
Japan, and #Hiroshima Univ., Higashi-Hiroshima, Japan
- 10:55 am Placing Substrate Contacts into Mixed-Signal**
15-5 Circuits Controlling Circuit Performance, A.
Hermann, M. Olbrich and E. Barke, University of Hannover,
Hannover, Germany
- 11:20 am Optimization of Phase-Locked Loop Circuits via**
15-6 Geometric Programming, D. Collieran, C. Portmann*,
A. Hassibi, C. Crusius, S. Mohan, S. Boyd**, T.H. Lee**
and M.d.M. Hershenson, Barcelona Design, Inc., Newark,
CA, *Aeluros, Inc., Mountain View, CA and **Stanford
University, Stanford, CA

Session 16 – Emerging Memory Circuits & Technology
Oak Ballroom, Tuesday Afternoon, September 23

Chair: Tom Andre Co-Chair: Cormac O'Connell

Novel circuit techniques for low-power, high-speed CAMs, adaptive I/Os and emerging memory technologies such as chalcogenide phase-change memory, FeRAMs and MRAMs are presented.

- 2:00 pm Introduction**
- 2:05 pm Pipelined Match-Lines and Hierarchical Search-**
16-1 Lines for Low-Power Content-Addressable
Memories, K. Pagiamtzis and A. Sheikholeslami,
University of Toronto, Toronto, Canada

- 2:30 pm** **200MHz/200MSPS 3.2W at 1.5V Vdd, 9.4Mbits Ternary CAM with New Charge Injection Match Detect Circuits and Bank Selection Scheme**, G. Kasai, Y. Takarabe, K. Furumi, M. Yoneda, SONY Corporation, Tokyo, Japan
- 2:55 pm** **Programmable and Automatically Adjustable On-Die Terminator for DDR3-SRAM Interface**, N.-S. Kim, Y.-J. Yoon, U.-R. Cho and H.-G. Byun, Samsung Electronics, Kyeonggi-Do, Korea
- 3:20 pm** **180nm Sn-Doped Ge₂Sb₂Te₅ Chalcogenide Phase-Change Memory Device for Low Power, High Speed Embedded Memory for SoC Applications**, Y. C. Chen, C.T. Chen, J.Y. Yu, C.Y. Lee, C.F. Chen, S.L. Lung and R. Liu, Macronix International Co., Taiwan, ROC
- 3:45 pm** **Break**
- 4:00 pm** **Resistance Ratio Read (R³) Architecture for a Burst Operated 1.5V MRAM Macro**, T. Inaba, K. Tsuchida, T. Sugibayashi**, S. Tahara** and H.Yoda*, Toshiba Corporation, Yokohama, Japan, *Toshiba Corporation, Kawasaki, Japan and **NEC Corporation, Kanagawa, Japan
- 4:25 pm** **Design and Applications of Ferroelectric Nonvolatile SRAM and Flip-Flop with Unlimited Read/Program Cycles and Stable Recall**, S. Masui, W. Yokozeki*, M. Oura, T. Ninomiya*, K. Mukaida*, Y. Takayama* and T. Teramoto*, Fujitsu Laboratories Limited, Tokyo, Japan and *Fujitsu Limited, Tokyo, Japan

<p>Session 17 – Nyquist-Rate Data Converters Fir Ballroom, Tuesday Afternoon, September 23</p>

Chair: David Naim Co-Chair: Richard Carley

This session covers the use of calibration, error cancellation and mismatch-insensitive techniques along with high-gain amplifiers and well controlled timing in the quest for accurate high speed analog signal processing.

- 2:00 pm** **Introduction**
- 2:05 pm** **A 12-bit 20-MS/s Pipelined ADC with Nested Digital Background Calibration**, X. Wang, P.J. Hurst and S. Lewis, University of California, Davis, CA
- 2:30 pm** **A 1.8-V 67mW 10-bit 100MSPS Pipelined ADC Using Time-Shifted CDS Technique**, J. Li and U.-K. Moon, Oregon State University, Corvallis, OR
- 2:55 pm** **A 16-Bit, 20MSPS CMOS Pipeline ADC with Direct INL Detection Algorithm**, S. Hisano and S. Sapp, Fairchild Semiconductor, Colorado Springs, CO
- 3:20 pm** **A 9b 165MS/s 1.8V Pipelined ADC with All Digital Transistors Amplifier**, M. Amourah, H. Bilhan*, F. Ying*, L. Fang*, G. Xu*, R. Chandrasekaran* and R. Geiger**, Barcelona Design, Inc., Newark, CA, *Texas Instruments, Dallas, TX, **Iowa State University, Ames, IA
- 3:45 pm** **Break**
- 4:00 pm** **Capacitor Matching Insensitive 12-bit 3.3 MS/s Algorithmic ADC in 0.25μm CMOS**, P. Quinn and M. Pribytko, Xilinx Ireland, Dublin, Ireland
- 4:25 pm** **A Dual 10b 200MSPS Pipeline D/A Converter with DLL-based Clock Synthesizer**, G.Manganaro, S.-U. Kwak and A. Bugeja, Engim Inc., Acton, MA

4:50 pm **A 10-b, 1-GSample/s Track-and-Hold Amplifier**
17-7 **Using SiGe BiCMOS Technology**, A. Razzaghi and M.
C. F. Chang, University of California, Los Angeles, CA

**Session 18 – Transmitters and Receivers for
Wireless Systems**

Pine Ballroom, Tuesday Afternoon, September 23

Chair: Earl McCune Co-Chair: Oliver Werther

These papers cover polar modulation and Cartesian feedback transmitters, a submicron CMOS transceiver, a direct-conversion receiver and a sigma-delta synthesizer.

2:00 pm **Introduction**

2:05 pm **Polar Modulator for Multi-mode Cell Phones,**
18-1 **(Invited)** W. Sander, S. Schell and B. Sander, Tropian, Inc.,
Cupertino, CA

2:55 pm **A 1V, 8GHz CMOS Integrated Phase Shifted**
18-2 **Transmitter for Wideband and Varying Envelope**
Communication Systems, S. Hamed-Hagh and C.A.T.
Salama, University of Toronto, Toronto, Canada

3:20 pm **Wide-Bandwidth Fully Integrated Cartesian Feed-**
18-3 **back Transmitter**, F. Carrara, A. Scuderi* and G.
Palmisano, Universita di Catania, Catania, Italy and
*STMicroelectronics, Catania, Italy

3:45 pm **Break**

4:00 pm **A CMOS Bluetooth Radio Transceiver Using a**
18-4 **Sliding-IF Architecture**, M. Chen*, K.H. Wang*, D.
Zhao*, L. Dai*, Z. Soe and P. Rogers, *Prominent
Communications, Inc., San Diego, CA

4:25 pm **A 15 mW, 70 kHz 1/f Corner Direct Conversion**
18-5 **CMOS Receiver**, E. Sacchi, I. Bietti, S. Erba*, L. Tee**,
P. Vilmercati and R. Castello#, STMicroelectronics, Pavia,
Italy, *STMicroelectronics, Cornaredo, Italy, **Univ. of
Calif., Berkeley, CA & #University of Pavia, Pavia, Italy

4:50 pm **An UMTS Sigma-Delta Fractional Synthesizer with**
18-6 **200kHz Bandwidth and -128dBc/Hz @ 1MHz Using**
Spurs Compensation and Linearization Tech-
niques, I. Bietti, E. Temporiti, G. Albasini and R.
Castello*, STMicroelectronics, Pavia, Italy and *University
of Pavia, Pavia, Italy

Session 19 – Custom Design & Applications

Cedar Ballroom, Tuesday Afternoon, September 23

Chair: Jamil Kawa Co-Chair: John Wright

Custom I/O and IP designers will appreciate the low-power and high-performance solutions discussed in this session, which also describes power generation, I/O communication, and IP optimization.

2:00 pm **Introduction**

2:05 pm **Proximity Communication**, R. Drost, R. Hopkins and I.
19-1 Sutherland, Sun Microsystems, Inc., Mountain View, CA

2:30 pm **A 2.2Gbps CMOS Look-Ahead DFE Receiver for**
19-2 **Multidrop Channel with Pin-to-Pin Time Skew**
Compensation, Y.-S. Sohn, S.-J. Bae, H.-J. Park, C.-H.
Kim* and S.-I. Cho*, Pohang Univ. of Science and Tech.,
Pohang, Korea and *Samsung Elec. Co., Hwasung, Korea

- 2:55 pm 19-3** **Integrated Circuit for High-Frequency Ultrasound Annular Array**, J. Talman, S. Garverick*, G. Lockwood**, The Cleveland Clinic Foundation, Cleveland, OH and *Case Western Reserve Univ. and **Queens Univ.
- 3:20 pm 19-4** **Bipolar Pulse Width Modulation Driver for MEMS Electrostatic Actuator Arrays**, S. Garverick, M. Nagy, M. Kane and J. Guo, Movaz Networks Inc., Norcross, GA
- 3:45 pm** **Break**
- 4:00 pm 19-5** **A 1/3" VGA Linear Wide Dynamic Range CMOS Image Sensor Implementing a Predictive Multiple Sampling Algorithm with Overlapping Integration Intervals**, P. Acosta-Serafini, I. Masaki and C. Sodini, Massachusetts Institute of Technology, Cambridge, MA
- 4:25 pm 19-6** **Piezoelectric Power Generation Interface Circuits**, T. Le, J. Han, A. von Jouanne, K. Mayaram and T. Fiez, Oregon State University, Corvallis, OR
- 4:50 pm 19-7** **A High Voltage Dickson Charge Pump in SOI CMOS**, M. Hoque, T. McNutt, J. Zhang, A. Mantooh and M. Mojarradi*, University of Arkansas, Fayetteville, AR and *Jet Propulsion Labs, Pasadena, CA

<p>Session 20 – Evening Panel Discussion</p>

<p>Oak Ballroom, Tuesday, September 23, 8:00 pm</p>

Technology: Falling Short of Product Developer Needs?

Organizers: Rich Liu, Macronix International
Larry Wissel, IBM Microelectronics

Moderator: John Abernathy, Director, ASIC Design Center,
IBM Microelectronics

Panelists:

Scott Crowder, Tech. Dev. Mgr
IBM Microelectronics

Jack Sun, Senior Dir.,
Logic Technology Division
TSMC

Erich Goetting, VP & GM,
Advanced Products Group
Xilinx

Simon Yang, VP
Technology Dev. Center
SMIC

Dan Lenoski, VP, Engineering
Routing Technology Group
Cisco

And a panelist from the CICC
audience!

We've been following Moore's Law down the VLSI highway for decades, reaping predictable performance and size benefits with every new technology generation. But the latest stretch of road, the introduction of 130nm technology, was full of bumps and detours. The next stretch doesn't look any better. Examples: as disappointing as the performance benefits of 130nm were, the performance benefits of 90nm and beyond are even more questionable. New gate dielectric materials are needed but not appearing. Leakage power, so long ignored, will limit future designs. Meaningful improvements in the metal-insulator dielectric constant have been elusive. Mask costs are exploding. What can product developers expect from technology suppliers in the future to satisfy consumers' needs?

In addition to the above well-known panelists, this year we are adding a panelist from the audience: one spot is reserved for a CICC attendee. To be filled when the panel begins. Attendees wanting to be a candidate for this panel spot will express their interests in advance, and prepare statements with their views on the panel issues. The panel audience will listen to all the candidates, and then vote to select the one who best represents the audience's views.

Session 21 – Evening Panel Discussion
Fir Ballroom, Tuesday, September 23, 8:00 pm

**Outsourcing! From Fabrication to Packaging, and now Design...
will the US Semiconductor Industry survive Overseas
Outsourcing?**

Organizers: Amjad Obeidat, National Semiconductor
Rakesh Kumar, TCX

Moderator: Rakesh Kumar, TCX

Panelists:

Behrooz Abdi, Vice President
Motorola

Werner Goertz, Vice President
WiPro

Mike Campbell, Vice President
Qualcomm

Ed Ross, President
TSMC USA

Brian Fitzgerald, CEO,
ChipWrights

Ann Lee Saxenian, Professor
University of California, Berkeley

The semiconductor industry witnessed a dramatic rise in the number of fabless companies in the 1990s. These companies based their business models on the basis of access to IC manufacturing processes at foundries such as TSMC and Chartered Semiconductor, and on access to assembly plants in South East Asia. In addition, as the cost of building fabs became an ever increasing percentage of corporate revenues, even traditional IC companies started to outsource part of their manufacturing and assembly to the same foundries. This trend shows no sign of slowing as both assembly and even design are being outsourced to overseas companies. These trends have serious consequences for the future of the IC industry in the US. Some of the main areas of interest and concern in this regard are:

- Foundry Support: Companies, including fabless ones, have to create groups that manage their relationships with the foundries with regards to obtaining updated models, up-to-date characterization data, lot tracking, etc. Such expertise is needed to ensure a successful product design and manufacturing cycle.

- Product Differentiation: With manufacturing process no longer a main differentiator, companies are looking for new ways to differentiate themselves from their competitors. Companies now look to distinguish their products through product features, power consumption, and manufacturing cost.

- Geological and Geopolitical Stability: With a significant number of foundries and assembly plants located in East Asia, a fabless company has to take into account what impact an earthquake or a regional instability such as war will have on its ability to deliver a product.

These topics will be considered and debated by our panel participants and the audience.

Session 22 – Evening Panel Discussion
Pine Ballroom, Tuesday, September 23, 8:00 pm

**Are (Analog) Device Models Really That Bad,
Or Are They Just A Convenient Excuse?**

Organizer/Moderator: Peter Kinget, Columbia University

Panelists:

Yu-Tai Chia, Dept. Mgr, SPICE
Modeling, TSMC

Ali Niknejad, Professor
University of California, Berkeley

Daniel Foty, President,
Gilgamesh Associates

Yannis Tsividis, Professor
Columbia University

Weidong Liu, Senior R&D Mgr.,
Mixed-Signal Simulation & TCAD
Synopsys

Pieter Vorenkamp, Sr. Director
Analog & RF :Micro-Electronics
Broadcom Corp.

Colin McAndrew, Director,
Enabling Technology
Motorola

The poor accuracy of device models is a constant complaint of circuit designers. Significant research has been done to improve device model equations which should alleviate these complaints. So, what is at the origin of this perpetual modeling debate?

Are the logistics of model extraction and parameter generation too complicated so that the most advanced tools are not available to product designers? Is the pace of technology change too fast for stable models to emerge? Is the nature of our industry that we constantly push (past) the limit, so that this problem will never go away? Maybe the advantage of good circuit models is not significant enough towards the product success so that management does not want to put resources in modeling. Or, are the models just an easy excuse for missed deadlines and requirements?

Session 23 – Bioelectronic Systems

Oak Ballroom, Wednesday Morning, September 24

Chair: Jim Lipman Co-Chair: Rahul Sarpeshkar

Advances in sensing and electronic circuits are fueling developments in biotechnology. See how recent innovations are benefiting the blind and deaf as well as enabling lab-on-chip bio-detection systems.

8:30 am Introduction

8:35 am Development of Microelectronic Based Biosensors
23-1 (Invited) A. Campitelli, C. Bartic, J-M. Friedt, K. De Keersmaecker, W. Laureyn, L. Francis, F. Frederix, G. Reekmans, A. Angelova, J. Suls, K. Bonroy, R. De Palma, Z. Cheng and G. Borghs, IMEC, Leuven, Belgium

9:25 am The Fabrication of Scalable Multi-Sensor Arrays
23-2 Using Standard CMOS Technology, M. Milgrew, D. Cumming and P. Hammond, University of Glasgow, Glasgow, Scotland

9:50 am Break

- 10:05 am 23-3 A Retinal Prosthesis Device Based on an 80x40 Hybrid Microelectronic-Microwire Glass Array, (Invited)** D. Scribner, L. Johnson, R. Klein, W. Bassett, J. Howard, P. Skeath, L. Wasserman, B. Wright, F. Perkins, M. Peckerar, B. Finch*, R. Graham*, C. Trautfield*, S. Taylor* and M. Humayun**, U.S. Naval Research Laboratory, Washington, DC, *Raytheon RVS Corporation, Goleta, CA and **Doheny Eye Institute, Los Angeles, CA
- 10:55 am 23-4 A 16-channel Analog VLSI Processor for Bionic Ears and Speech-Recognition Front Ends, (Invited)** M. Baker, T.K.-T. Lu, C. Salthouse, J.-J. Sit, S. Zhak and R. Sarpeshkar, Mass. Institute of Technology, Cambridge, MA

Session 24 – Interconnect Schemes for Multi-GHz RF

Fir Ballroom, Wednesday Morning, September 24

Chair: Rich Liu Co-Chair: Jeff Babcock

This session presents both on-chip and system-in-package interconnect schemes suitable for improving the performance of RF circuits. New innovations using surface-mount techniques, post-passivation metallization, and organic substrates are discussed.

- 8:30 am Introduction**
- 8:35 am 24-1 A Surface-Mounted RF IC Technology Demonstrated with a 10 GHz LC Oscillator with Copper Coils,** J. van der Tang, R. Dekker* and A. van Roermund, University of Technology, Eindhoven, The Netherlands and *Philips Research Labs, Eindhoven, The Netherlands
- 9:00 am 24-2 A New IC Interconnection Scheme and Design Architecture for High Performance ICs at Very Low Fabrication Cost - Post Passivation Interconnection,** M. S. Lin, L. Chen, J.Y. Lee, H.T. Liu, C.K. Chou, K.H. Wan, H.M. Chen, K. Chou, R. Hsiao and E. Lin, Megic Corp, Hsin-Chu, Taiwan
- 9:25 am 24-3 Silicon-on-Organic Integration of a 2.4GHz VCO Using High Q Copper Inductors and Solder-Bumped Flip Chip Technology,** X. Huo, G.-W. Xiao, K.J. Chen and P.C.H. Chan, Hong Kong University of Science and Technology, Hong Kong, China
- 9:50 am Break**

Session 25 – RF & Microwave LO Generation Techniques

Pine Ballroom, Wednesday Morning, September 24

Chair: Ali Niknejad Co-Chair: Francesco Svelto

These papers cover VCO design tradeoffs with specific emphasis on low-phase noise, wide tuning range, and digital control and calibration. Injection locking techniques for quadrature generation are also presented.

- 8:30 am Introduction**
- 8:35 am 25-1 Lumped, Inductorless Oscillators: How Far Can They Go?,** R. Navid, T.H. Lee and R. Dutton, Stanford University, Stanford, CA
- 9:00 am 25-2 The Impact of Device Type and Sizing on Phase Noise Mechanisms,** A. Jerng and C. Sodini, Massachusetts Institute of Technology, Cambridge, MA

- 9:25 am 25-3** **A 0.35-V 1.46-mW Low-Phase-Noise Oscillator with Transformer Feedback in Standard 0.18- μ m CMOS Process**, K. Kwok and H.C. Luong, Hong Kong Univ. of Science and Technology, Clear Water Bay, Hong Kong
- 9:50 am** **Break**
- 10:05 am 25-4** **A Wideband Low-Phase-Noise CMOS VCO**, A. Berny, A. Niknejad and R. Meyer, University of California, Berkeley, CA
- 10:30 am 25-5** **A 2-GHz Wide Band Low Phase Noise Voltage-Controlled Oscillator with On-Chip LC Tank**, J.-K. Cho, H.-I. Lee, K.-S. Nah and B.-H. Park, Samsung Electronics, Kyounggi-Do, Korea
- 10:55 am 25-6** **Injection Locking LC Dividers for Low Power Quadrature Generation**, A. Mazzanti, P. Uggetti*, P. Rossi* and F. Svelto*, Universita di Modena e Reggio Emilia, Modena, Italy and *University of Pavia, Pavia, Italy
- 11:20 am 25-7** **A Subharmonically-Injected Quadrature LO Generator for 17GHz WLAN Applications**, D.K. Ma, J. Long* and D. Harnam**, University of Toronto, Ontario, Canada, *Delft University of Technology, Delft, The Netherlands and **IBM Microelectronics, Burlington, VT
- 11:45 am 25-8** **Just-In-Time Gain Estimation of an RF Digitally-Controlled Oscillator**, R. Staszewski, D. Leipold, J. Wallberg and P. Balsara*, Texas Instruments Inc, Dallas, TX and *University of Texas, Richardson, TX

<p align="center">Session 26 – Broadband Wired Communication Systems Cedar Ballroom, Wednesday Morning, September 24</p>

Chair: Amjad T. Obeidat Co-Chair: Johan Van Der Tang

This session covers advancements and future trends in broadband communication links and interface I/Os focusing on ultra-high data rates, low power, and innovations for increasing channel capacity.

- 8:30 am** **Introduction**
- 8:35 am 26-1** **A Low-Power 0.13 μ m CMOS OC-48 SONET and XAU1 Compliant SERDES**, R. Wadhwa, A. Aggarwal, J. Edwards, M. Ehlert, J. Hoehn, G. Miao, K. Lakshmikummar and J. Khoury, Multilink Technology Corp., Somerset, NJ
- 9:00 am 26-2** **A 39.8Gb/s to 43.1Gb/s SFI-5 Compliant 16:1 Multiplexer and 1:16 Demultiplexer for Optical Communication Systems**, T. Krawczyk, S. Steidl, R. Alexander, J. Pulver, G. Kowalski, C. Hombuckle and D. Rowe, Sierra Monolithics Inc., Redondo Beach, CA
- 9:25 am 26-3** **A 62.5Gb/s Multi-Standard SerDes IC**, H. Partovi, B. Evans*, T. Wilson*, S. Shelton*, E. Naviasky*, E. Sanjeevi, Y. Wen, K. Gopalakrishnan, S. Chokkalingam, H. Thompson*, M. Casas*, L. Ye*, M. Hufford*, Y. Qiu, M. Williams*, J. James*, A. Baldisserotto*, S. White*, S. Williams*, D. Georgantas* and T. Gray*, Infineon Tech., San Jose, CA, & *Cadence Design Foundry, Columbia, MD
- 9:50 am** **Break**
- 10:05 am 26-4** **Modeling and Analysis of High-Speed Links. (Invited)** V. Stojanovic**,** and M. Horowitz*, *Stanford University, Stanford, CA and **Rambus Inc, Los Altos, CA

10:55 am 26-5 A Fully-Integrated 10.5 to 13.5 Gbps Transceiver in 0.13 μ m CMOS, G. Miao, P. Ju, D. Ng, J. Khoury and K. Lakshmikummar, Multilink Technology Corp., Somerset, NJ

11:20 am 26-6 A Universal Quad AFE with Integrated Filters for VDSL, ADSL, and G. SHDSL, N. Tan, F. Caster, C. Eichrodt, S. George, B. Horng and J. Zhao, GlobeSpan Virata, Inc., Irvine, CA

Session 27 – Towards Testing in the 90-Nanometer Era

Fir Ballroom, Wednesday Morning, September 24

Chair: Mike Zachariah Co-Chair: Frank Bouwman

Pushing into the 90-nanometer era gives rise to new failure mechanisms, requiring new analysis and test-measurement techniques. This session includes a tutorial on nanometer CMOS failure mechanisms, case studies, and a description of a 10 GHz on-chip sampling oscilloscope circuit.

10:00 am Introduction

10:05 am 27-1 CMOS IC Nanometer Technology Failure Mechanisms, (Invited) C. Hawkins, A. Keshavarzi* and J. Segura**, University of New Mexico, *Intel Corporation and **University of Balearic Islands

10:55 am 27-2 In-System Failure Investigation on 0.18 μ m High Speed Serial Link ASIC using Logic Built-in Self Test, J. Mechler, R. Bulaga and J. Garlett, IBM, Essex Junction, VT

11:20 am 27-3 Measurements and Analysis of SER Tolerant Latch in a 90nm dual-Vt CMOS Process, P. Hazucha, T. Karnik, S. Walstra, B. Bloechel, J. Tschanz, J. Maiz, K. Soumyanath, G. Dermer, S. Narendra, V. De and S. Borkar, Intel Corporation, Hillsboro, OR

11:45 am 27-4 A 5-Channel, Variable Resolution, 10-GHz Sampling Rate Coherent Tester/Oscilloscope IC and Associated Test Vehicles, M. Hafed and G. Roberts*, DFT Microsystems Inc., Quebec, Canada and *McGill University, Quebec, Canada

Session 28 – Low Power Circuits and Techniques

Oak Ballroom, Wednesday Afternoon, September 24

Chair: Tadahihiro Kuroda Co-Chair: Takayasu Sakurai

Advanced process technologies make power consumption a significant issue. This session presents advanced circuit techniques for power reduction.

1:30 pm Introduction

1:35 pm 28-1 Estimation of Iddq for Early Chip and Technology Design Decisions, T. Hook, L. Wissel and D. Mazgaj, IBM Microelectronics, Essex Junction, VT

2:00 pm 28-2 An Ultra-Low-Power, Radiation-Tolerant Reed Solomon Encoder for Space Applications, J. Gambles, L. Miles, J. Hass, W. Smith, S. Whitaker and B. Smith*, Univ. of Idaho, Post Falls, ID and *PicoDyne, Inc., Annapolis, MD

- 2:25 pm 28-3** **Statistical Leakage Current Reduction by Self-Timed Cut-Off Scheme for High Leakage Environments**, J.-H. Choi and T. Sakurai, University of Tokyo, Tokyo, Japan
- 2:50 pm** **Break**
- 3:05 pm 28-4** **Standby Voltage Scaling for Reduced Power**, B. Calhoun and A. Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA
- 3:30 pm 28-5** **A High-Speed and Low-Voltage Associative Co-Processor With Hamming Distance Ordering Using Word-Parallel and Hierarchical Search Architecture**, Y. Oike, M. Ikeda and K. Asada, University of Tokyo, Tokyo, Japan
- 3:55 pm 28-6** **Resonant Clocking Using Distributed Parasitic Capacitance**, A. Drake, K. Nowka*, T. Nguyen*, J. Burns* and R. Brown, University of Michigan, Ann Arbor, MI and *IBM Austin Research Lab, Austin, TX

Session 29 – SoC Design Challenges and Trade-Offs

Fir Ballroom, Wednesday Afternoon, September 24

Chair: Iraj Masarati Co-Chair: Thomas Zimmermann

This session encapsulates SoC considerations in hardware and embedded software; system-on-programmable-chip; and design challenges and trade-offs for system-in-package versus system-on-chip.

- 1:30 pm** **Introduction**
- 1:35 pm 29-1** **Embedded Software in the SoC World. How HdS Helps to Face the HW and SW Design Challenge (Invited)** F. Pospiech and S. Olsen*, Alcatel, Paris, France and *Mentor Graphics, San Jose, CA
- 2:25 pm 29-2** **Architecture and Methodology of a SoPC with 3.25Gbps CDR based Serdes and 1Gbps Dynamic Phase Alignment**, R. Venkata, W. Wong, T. Tran, V. Chan, T. Hoang, H. Lui, B. Ton, S. Shumurayev, C. Lee, S. Wang, H. Ngo, M. Kabani, V. Maruri, T. Lai, T. Nguyen, A. Zaliznyak, M. Luo, T. Nguyen, K. Asaduzzaman, S. Maangat, J. Lam and R. Patel, Altera Corp., San Jose, CA
- 2:50 pm** **Break**
- 3:05 pm 29-3** **Design Challenges for System-In-Package vs System-On-Chip**, C. Trigas, Motorola Semiconductor Product Sector, Munich, Germany
- 3:30 pm 29-4** **A Feasibility Study of 2.5D System Integration**, Y. Deng and W. Maly, Carnegie Mellon Univ., Pittsburgh, PA
- 3:55 pm 29-5** **A Distributed Crossbar Switch Scheduler for On-Chip Networks**, K. Lee, S.-J. Lee and H.-J. Yoo, KAIST, Daejeon, Korea

Session 30 – Analog Techniques

Pine Ballroom, Wednesday Afternoon, September 24

Chair: Jose Cruz-Albrecht Co-Chair: Takahiro Miki

This session covers the design of low-voltage operational amplifiers and a buffer, along with techniques for switching-noise reduction and for capacitance multiplying.

- 1:30 pm** **Introduction**

- 1:35 pm** **Low-Voltage Power-Efficient Operational Amplifier Design Techniques - An Overview, (Invited)** K.-J. de Langen and J. H. Huijsing*, Philips Semiconductors, San Jose, CA and *Delft Univ. of Tech., Delft, The Netherlands
- 2:25 pm** **A Highly Linear CMOS Buffer Circuit with an Adjustable Output Impedance**, M. Koutani, Y. Fujimoto and M. Miyamoto, Sharp Corporation, Nara, Japan
- 2:50 pm** **Break**
- 3:05 pm** **A High-Frequency 750mV Operational Amplifier in a Standard Bulk CMOS Process**, Y. Tang and R. Geiger, Iowa State University, Ames, IA
- 3:30 pm** **Switching Noise Reduction Techniques for Switched-Capacitor Voltage Doubler**, H. Lee and P.K.T. Mok, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong
- 3:55 pm** **A New Method for Multiplying the Miller Capacitance Using Active Components**, G. de Cremoux, Y. Christoforou and I. van Loo, Philips Semiconductors, Nijmegen, The Netherlands

<p>Session 31 – Noise Modeling Cedar Ballroom, Wednesday Afternoon, September 24</p>

Chair: Yuhua Cheng Co-Chair: Albert Stritter

These papers cover noise-modeling techniques for various applications such as power-line noise reduction and phase-noise analysis.

- 1:30 pm** **Introduction**
- 1:35 pm** **An Equation-based Method for Phase Noise Analysis**, B. Limketkai and R. Brodersen, University of California, Berkeley, CA
- 2:00 pm** **Efficient Generation of $1/f^2$ Noise Using a Multi-Rate Filter Bank**, J. Park, K. Muhammad* and K. Roy, Purdue University, West Lafayette, IN and *Texas Instruments Inc., Dallas, TX
- 2:25 pm** **Modeling of Jitter in Bang-Bang Clock and Data Recovery Circuits**, J. Lee, K. Kundurt* and B. Razavi, University of California, Los Angeles, CA and *Cadence Design Systems, San Jose, CA
- 2:50 pm** **Break**
- 3:05 pm** **Theoretical Study of Stubs for Power Line Noise Reduction**, T. Nakura, M. Ikeda and K. Asada, University of Tokyo, Tokyo, Japan
- 3:30 pm** **Noise Analysis Methodology for Partially Depleted SOI Circuits**, M. Nanua and D. Blaauw*, Motorola Semiconductor Products Sector, Austin, TX and *University of Michigan, Ann Arbor, MI
- 3:55 pm** **On-Package Decoupling Optimization with Package Macromodels**, H. Zheng, B. Krauter* and L. Pileggi, Carnegie Mellon University, Pittsburgh, PA and *IBM Corporation, Austin, TX

GENERAL INFORMATION

LOCATION DoubleTree Hotel
2050 Gateway Place
San Jose, CA 95110
(408) 453-4000
www.doubletree.com

REGISTRATION

Payment of the Technical Session registration fee entitles the registrant to entrance to all Monday-Wednesday, Technical Sessions, the Exhibit Hall, Exhibitor Preview Sessions, Exhibitor's Reception, Tuesday Happy Hour and one copy of the Conference Proceedings. Single-day registration entitles the registrant to that day's events and one copy of the Conference Proceedings. Technical session registration does not include entrance to the Sunday Educational Sessions.

Payment of the Sunday Educational Sessions registration fee entitles the registrant to entrance to the Sunday Educational Sessions, lunch on Sunday, and one copy of the Educational Sessions Workbook. Educational Session registration does not include entrance to the Monday-Wednesday Technical Sessions, the Exhibits or a copy of the Conference Proceedings.

To register online for the Technical Sessions and/or Sunday Educational Sessions go to the CICC website at www.ieee-cicc.org. Click on Registration.

To register by fax or mail fill out the registration form in the center of this booklet and fax or mail the form and payment to be received by **September 8**.

Don't register online and by mail or fax –it will result in double billing!

**Online and mail/fax registration forms MUST be received by
Monday, September 8**

After that date please register onsite at the conference.

Make checks payable to CICC 2003 in US dollars on a US bank. We also accept **VISA** and **MasterCard only**. CICC is not able to accept American Express charges. Requests for cancellations must be received by September 8, 2003 to qualify for a refund.

The Registration Center, located in the Bayshore Foyer, will be open as follows:

Registration for Sunday Educational Sessions Only

Sunday, Sept. 21 7:00 am - 2:00 pm

Registration for Technical Sessions

Sunday, Sept. 21 2:00 pm - 5:00 pm

Monday, Sept. 22 7:30 am - 5:00 pm

Tuesday, Sept. 23 8:00 am - 5:00 pm

Wednesday, Sept. 24 8:00 am - 3:00 pm

HOTEL ACCOMMODATIONS

The DoubleTree Hotel is located at 2050 Gateway Place, San Jose, California. The hotel has an outdoor swimming pool and exercise facilities. Parking at the Hotel is free. The hotel is only 1 mile from the San Jose Airport.

The room rate is \$169 for a single or double room. All rooms must be guaranteed with a credit card. To make a hotel reservation call the hotel at (408) 453-4000 or go to the CICC website www.ieee-cicc.org, click on Hotel Reservations, then complete the form.

You will receive a reservation confirmation directly from the hotel. It is the responsibility of each participant to make changes or cancellations directly with the hotel no later than 24 hours prior to scheduled arrival. No refunds will be given by the hotel for changes or cancellations with less than 24 hours notification.

EDUCATIONAL SESSIONS

On Sunday, Sept. 21, the CICC sponsors four Educational Sessions.

These Sessions are:

1. Advanced RF: From Devices to Systems
2. Advanced Data Converter Design and Test Techniques
3. High-Performance & Low-Voltage Design Challenges & Techniques
4. Hands on for SoC/Mixed-Signal/RF: Design, Verification and Test

To register, complete the Advance Registration Form for receipt by **Sept. 8**

EXHIBITORS' RECEPTION

Monday Evening, Sept. 22, 5:30 pm - 8:00 pm

Donnor Ballroom

The CICC social event this year is an Exhibitors' Reception sponsored by the CICC 2003 Exhibits Committee, held in the Exhibit Hall. All conference attendees are cordially invited! Enjoy the evening by browsing around the exhibit area, talking with the exhibitors' staff, seeing old friends and meeting new ones. Join us at the Exhibitors' Reception to celebrate CICC's 25th Anniversary!

CICC LUNCHEON

Tuesday, Sept. 23, 12:00 pm - 1:30 pm

Sierra Ballroom

Chips and Robots

Dr. Tsugio Makimoto

Corporate Advisor, Sony Corporation

The historical review of robots, from the first generation to the fourth generation, will briefly be presented. Following this review will be the story of Sony's entertainment robots including a dog-like robot, AIBO, and a biped humanoid robot. The critical roles played by chip technology will be discussed. It will be emphasized that robots will continue providing never-ending challenges for chip engineers and will become a new "technology driver" in the coming decades. -----

Dr. Makimoto is Corporate Advisor and Co-Chief Technology Officer of Micro Systems Network Company, Sony Corporation. Dr. Makimoto has devoted his career in the field of semiconductors more than 40 years. He received the B.S. degree from the University of Tokyo in 1959, the M.S. degree in 1966 from Stanford University., and the Ph.D. degree from the University of Tokyo in 1971. From 1959 to 1999, he worked in the Semiconductor Division of Hitachi Ltd. In the late 1970s, he was responsible for high-speed CMOS devices that marked a key turning point in the history of the semiconductor industry.



In the 1980s, Dr. Makimoto discovered the cyclical nature of the semiconductor industry which alternates directions between customization and standardization, roughly every ten years. This cycle was named "Makimoto's Wave" by Electronics Weekly in the UK. Based on this wave concept, he wrote a book "Living with the Chip" in 1995 jointly with D. Manners. In the 1990s, he took leadership in developing and manufacturing high-density DRAMs and new types of RISC microprocessors, and was nominated an IEEE FELLOW in 1997 for his contribution for developing and manufacturing high-density MOS devices. In 1997, he wrote a book titled "Digital Nomad", again with D. Manners, to introduce the new trends in the field of electronics after the PC. Dr. Makimoto gave a plenary talk at the last IEDM on chip technologies for entertainment robots.

EVENING PANEL DISCUSSIONS

On Tuesday evening, Sept. 23, beginning at 8:00 pm, the CICC will offer three evening panel discussions on timely issues:

1. Outsourcing! From Fabrication to Packaging, and now Design – will the U.S. semiconductor industry survive overseas outsourcing?
2. Are Analog Device Models Really that Bad or are they just a Convenient Excuse?
3. Technology: Falling Short of Product Developer Needs?

CONFERENCE PROCEEDINGS

The proceedings contains papers on each presentation. Technical Session registrants will receive one copy of the Proceedings. Additional copies will be available at the conference registration desk. IEEE member: \$80, Non-member: \$90. After the conference, order the Proceedings through: Single Copy Sales, IEEE Service Center, 445 Hoes Lane, Box 1331, Piscataway, NJ, 08855-1331, Customer Service Department (toll free): 800-678-4333. The IEEE catalogue number is 03CH37448.

AUTHOR INTERVIEWS

There will be author interviews each day of the conference immediately following the afternoon sessions in Gateway Foyer. This additional forum provides an opportunity for relaxed discussions with your colleagues outside the strict time constraints of the regular sessions.

SPONSOR EVENTS

CICC acknowledges the generous support of our conference sponsors
AMI for the T-Shirts
Synopsys for the Tote Bag
Tanner EDA for the Lanyards

AIRPORT TRANSPORTATION

The DoubleTree Hotel is approximately 1 mile from San Jose Airport. There is a complementary hotel shuttle from San Jose Airport to the hotel that runs from 6:00 am to midnight. Call the hotel on the DoubleTree Courtesy Phone outside the baggage area at San Jose Airport.

For passengers flying into San Francisco Airport, the San Jose Doubletree is approximately 33 miles from the airport. Supershuttle Service provides shuttle service from the airport to the hotel. Arrangements can be made at Ground Transportation or by calling (415) 558-8500 for more information. The cost is \$38.00/one way or \$76.00/round-trip. Taxi service is also available from the airport at an estimated cost of \$75.00.

BADGES

Badges are required for admittance to all sessions and the exhibit hall. Please wear your badge at all times while attending the conference so that you will not be delayed entry to a session.

FOR FURTHER INFORMATION CONTACT

CICC 2003
Suite 312
16220 S. Frederick Ave.
Gaithersburg, MD 20877
Phone: 301-527-0900 ext. 101, Fax: 301-527-0994
Email: cicc@his.com
Home Page: <http://www.ieee-cicc.org>

2003 STEERING COMMITTEE

Mike Beunder, Cavendish Kinetics **Jeff Oppold**, IBM Microelectronics
Phil Diodato, Agere Systems **Larry Starr**, Intel Corporation
Brian Fitzgerald, ChipWrights, Inc. **Trudy Stetzler**, Texas Instruments
Rakesh Kumar, TCX Inc.

2003 ORGANIZING COMMITTEE

General Chair Phil Diodato, Agere Systems	Panel Chair Jafar Savoj, Marvell Semicond.
Conference Chair Larry Starr, Intel Corporation	Special Events Chair John Wright, AMI Semicond.
Technical Program Chair Trudy Stetzler, Texas Instruments	Publicity Chair Ann Rincon, AMI Semicond.
Educational Sessions Chair Doug Garrity, Motorola	At-Large Member Jim Lipman, Elec. Industry Consultant Rakesh Kumar, TCX Inc.
Exhibits Chair Jackie Snyder, SliceX	Treasurer Mike Beunder, Cavendish Kinetics

2003 TECHNICAL PROGRAM COMMITTEES

Analog Circuit Design

Chair: Doug Garrity, Motorola
Co-Chair: Jose Cruz-Albert, HRL Laboratories, LLC

David Allee , Arizona State Univ.	Takahiro Miki , Renesas Technology Corp.
Rick Carley , Carnegie Mellon Univ.	David Nairn , Analog Devices Inc.
Yusuf Haque , Maxim Integrated Products	Pat Rakers , Motorola Labs Don Thelen , AMI Semiconductor

Custom Application and Low-Power Circuits Techniques

Chair: Kenneth Szajda, LSI Logic
Co-Chair: Takayasu Sakurai, University of Tokyo

Jamil Kawa , Synopsys	Jackie Snyder , SliceX
Tadahiro Kuroda , Keio University	John Wright , AMI Semiconductor

Signal & Data Processing

Chair: Ram Krishnamurthy, Intel Corp.
Co-Chair: Dawn Fitzgerald, ChipWrights, Inc.

Bryan Ackland , Agere Systems	Khurram Muhammad , Intel Corp.
Masataka Matsui , Toshiba Corp.	

Embedded Memory

Chair: Sreedhar Natarajan, ATMOS Corporation
Co-Chair: Kenji Noda, NEC Electronics

Tom Andre , Motorola	Cormac O'Connell , SiGe Microsystems
Phil Diodato , Agere Systems	Jeff Oppold , IBM Microelectronics Semiconductor Co.
Shinji Miyano , Toshiba Corp.	

Emerging Technologies

Chair: Jim Lipman, Elec. Industry Consultant
Co-Chair: Ann Rincon, AMI Semiconductor, Inc.
Rakesh Kumar, TCX Inc. **Albert Wang**, Illinois Institute of Technology
Rahul Sarpeshkar, MIT
Larry Star, Intel Corporation

Fabrication

Chair: David Sunderland, Boeing Satellite Systems
Co-Chair: Rich Liu, Macronix International Co., Ltd.
Jeff Babcock, Cree Microwave **Sanford Chu**, Chartered Semiconductor
C. S. Chang, TSMC **Larry Wissel**, IBM Microelectronics

Programmable Devices

Chair: Vaughn Betz, Altera
Co-Chair: Steve Wilton, University of British Columbia
Trevor Bauer, Xilinx **Brian Fitzgerald**, ChipWrights, Inc.

Simulation and Modeling

Chair: L. W. Nagel, Omega Enterprises
Co-Chair: Colin McAndrew, Motorola
Yuhua Cheng, Skyworks Solutions **Steffen Rochel**, Simplex Solutions
Elliot Gould, C-Port Corp. **Albert Stritter**, Infineon Tech. AG
Hidetoshi Onodera, Kyoto Univ. **Hong-Ha Vuong**, Agere Systems

SoC-IP/IC Generation and Management

Chair: Michele Taliercio, Accent S.r.l.
Co-Chair: Ric Williams, Sun Microsystems
Mike Beunder, Cavendish Kinetics **Rakesh Patel**, Altera Corp.
Henry Chang, Cadence Design Systems **Michael Reinhardt**, Rubicad Corp.
Iraj Masarati, SiRF **Thomas Zimmermann**, Motorola

Test and Reliability

Chair: Gordon Roberts, McGill University
Co-Chair: Mike Zacharia, Intel Corporation
Frank Bouwman, Philips Semiconductors **Gordon Roberts**, McGill University
Mike Zacharia, Intel Corporation

Wired Designs

Chair: Sang-Soo Lee, LSI Logic
Co-Chair: Vincent Von Kaenel, Broadcom Corporation
Herman Casier, Alcatel Microelectr. **Dave Rich**, Lafayette College
Kumar Lakshmikummar, Multilink Tech. Corp. **Jafar Savoj**, Marvell Semiconductor
Un-Ku Moon, Oregon State Univ. **Johan Van Der Tang**, Eindhoven University of Technology
Amjad Obeidat, Nat'l Semicond.

Wireless Designs

Chair: Peter Kinget, Columbia University
Co-Chair: Oliver Werther, Microtune
Jean-Baptiste Begueret, Univ. of Bordeaux **Earl McCune**, Tropian
Andrea Boni, University of Parma **Ali Niknejad**, Univ. of California, Berkeley
Edoardo Charbon, EPFL **Trudy Stetzler**, Texas Instruments
Stefan Drude, Philips Semicond. **Francesco Svelto**, Univ. of Pavia
Noboyuki Itoh, Toshiba